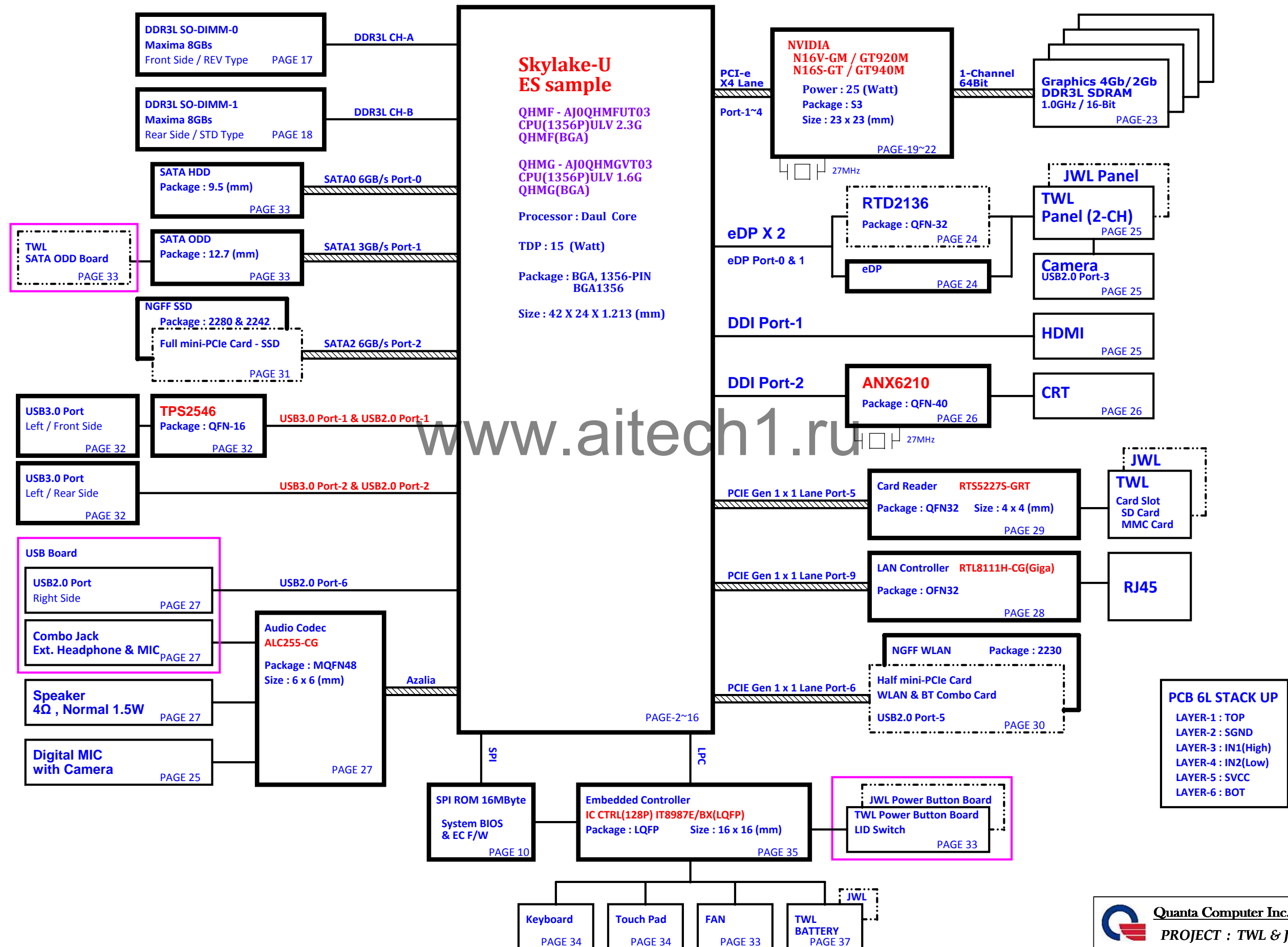
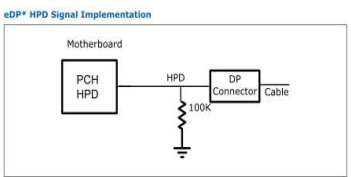
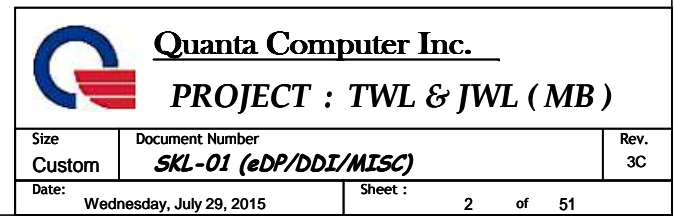
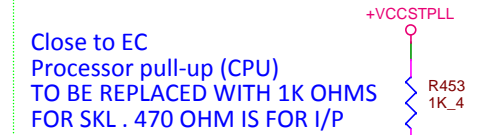


TWL + JWL Intel SKYLAKE-U Platform Block Diagram





PLACE NEAR CPU



The image displays two detailed PCB layout diagrams for a DDR3 memory module, labeled U25B and U25C. Each diagram shows a top layer (SKL_ULT) and a bottom layer (SKL_ULT) with various components and traces. The diagrams include component footprints, pin numbers, and labels for different signal groups (A0, A1, B0, B1, A2, A3, B2, B3). A large watermark 'www.aitech.com' is visible across the center of the diagrams. The diagrams are labeled 'REV = 1' and '2 OF 20'.



PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

[16,19,26,28,29,30,33,35]

PLTRST#

[16] SYS_RESET#

[35] RSMRST#

R264
100K/F_4EC72
*220P/50V_4X1B-1218 Reserve
PU with +VCCSTPLL

+1.0V

+VCCSTPLL

R459
1K_4R458
*1K_4R499
*10K_4C703
*10P/50V_4

H VCCST_PWRGD R

R457
60.4_4Close to CPU side
H_VCCST_PWRGD
trace length 0.3" - 1.5"

System PWR_OK(CLG)

[16] SYS_PWROK

[16,35] EC_PWROK

[35] DSWROK_EC

[35] SUSWARN#_EC

[35] SUSACK#_EC

[28,29,30,35] PCIE_WAKE#

[3,18] DDR_VTT_CNTL

Need check circuit!!!!
Should be deleteU25K
SKL_ULT
SYSTEM POWER MANAGEMENT

PLTRST# AN10

SYS_RESET# B5

RSMRST# AY17

PROC_PWRGD A68

H_VCCST_PWRGD B65

SYS_PWROK B6

EC_PWROK BA20

DSWROK_EC R BB20

SUSWARN# AR13

SUSACK# AP11

PCIE_WAKE# BB15

LAN_WAKE# AM15

DDR_VTT_CNTL AT15

GPP_B12/SLP_S0#

GPD4/SLP_S3#

GPD5/SLP_S4#

GPD10/SLP_S5#

SLP_SUS#

SLP_LAN#

GPD9/SLP_WLAN#

GPD6/SLP_A#

GPD3/PWRBTN#

GPD1/ACPRESENT

GPD0/BATLOW#

GPP_A11/PME#

INTRUDER#

GPP_B11/EXT_PWR_GATE#

GPP_B2/VRALERT#

WAKE#

GPD2/LAN_WAKE#

GPD11/LANPHYPC

GPD7/RSVD

*SKL_ULT

REV = 1 11 OF 20

PCH Pull-high/low(CLG)

SUSWARN# R285 *10K_4

SUSACK# R281 10K_4

WLAN_OFF_PCH R258 10K_4

20150521A-X1B SUSWARN# abnormal waveform.
SUSWARN# isn't OD. Remove pull high resistor.

X1B-1127 PU resistor for SUSACK# change to stuff.

PCIE_WAKE# R563 1K_4

AC_PRESENT_EC R564 *10K_4

LAN_WAKE# R606 *10K_4

20150520A-X61 auto-wake issue.
LAN_WAKE# need to be pull high +3VPCU or +3VS5.
(LAN_WAKE# need pull high DSW power plane.
Commercial is +3VPCU, but consumer is +3VS5.)

SYS_RESET# R443 10K_4

RSMRST# R569 10K_4

DSWROK_EC R570 100K/F_4

Figure 43-1. SKL U/Y Flow Diagram for SYS_PWROK/PCH_PWROK Generation

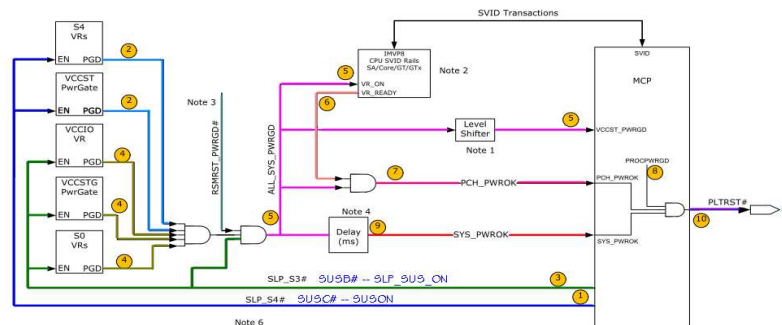
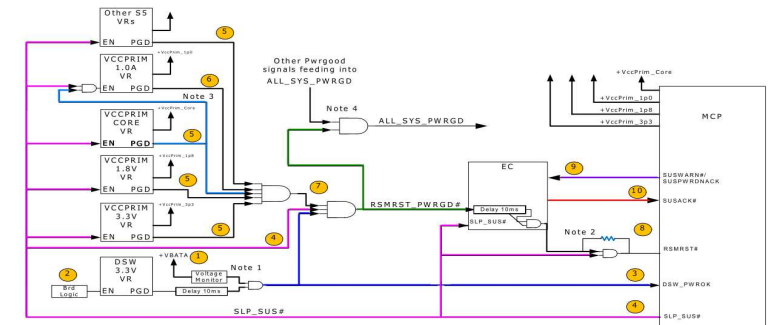


Figure 43-2. SKL U/Y Flow Diagram for RSMRST_PWRGD# Generation



+1.0V	[2,6,16,32,35,41]
+3V	[2,10,11,12,13,14,15,16,17,18,19,21,22,24,25,26,27,28,29,30,31,33,34,35,36,42,44,45,46]
+3V_DEEP_SUS	[10,11,12,14,15,16,18]
+3V_RTC	[13,15,32]
+3VS5	[10,15,16,27,30,33,35,36,38,40,41,44,47]
+5VS5	[27,32,36,38,39,40,41,42,43,44,45,46,47]
+VCCSTPLL	[2,5,6,9,41,42]

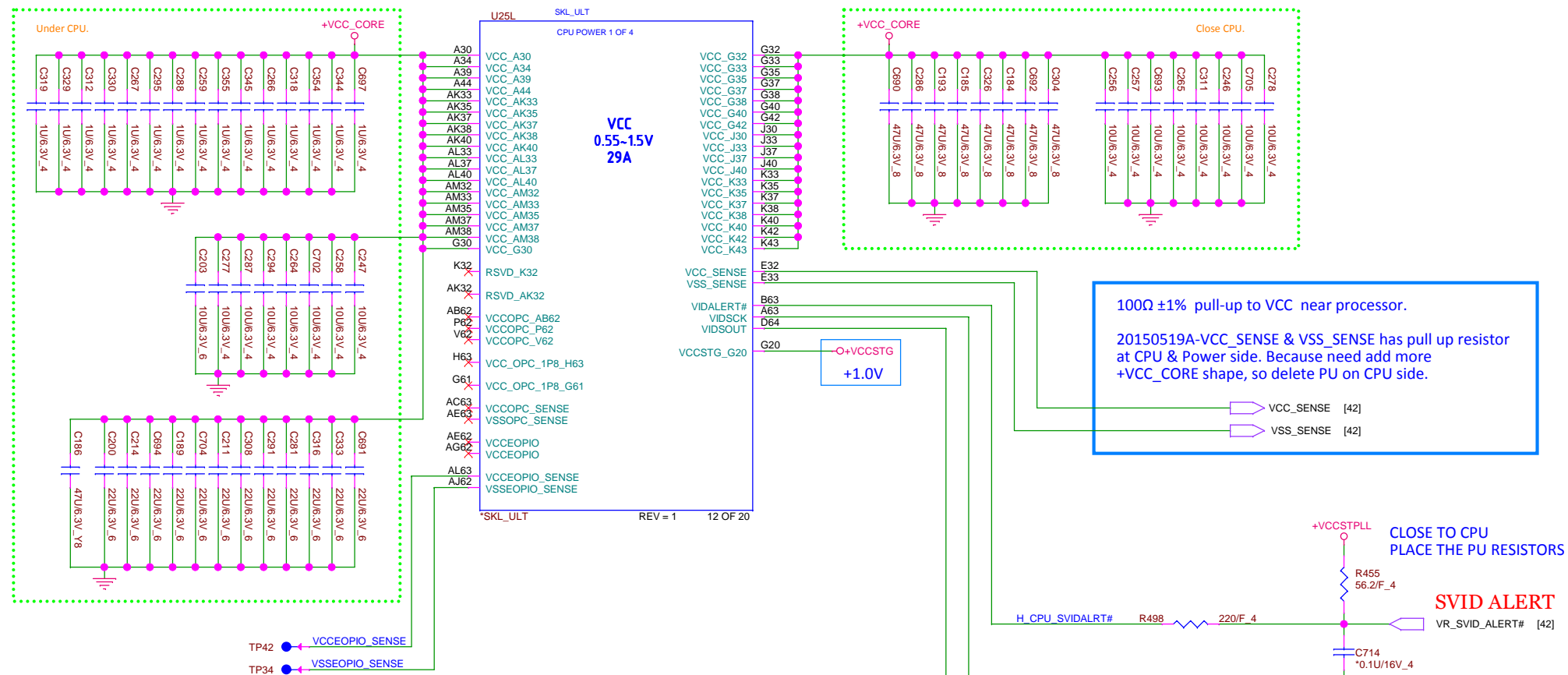
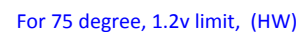
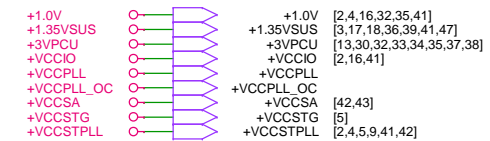


Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note ¹
Operating Voltage	Voltage Range for Processor Active Operating Mode	All	0.55	—	1.5	V	1,2,3,7,12
Idle Voltage	Voltage Range for Processor Idle Mode (Package C6/C7)	All	0	—	0.55	V	1,2,3,7
I _{CCMAX} CPU Core Power	Maximum Processor IA Core I _{CC}	Y(4W)	—	TBD	24	A	4,6,7,11
		U(15W)-dual core GT ₂	—	TBD	29		
		U(15W)-dual core GT ₃ +OPC	—	TBD	29/35 ¹⁴		
		U(28W)-dual core GT ₃ +OPC	—	TBD	29/35 ¹⁴		
		H(35W)-quad core GT ₂	—	TBD	60		
		H(45W)-quad core GT ₂	—	TBD	68		
		H(35W)-quad core GT ₄ +OPC	—	TBD	57		
		H(45,65W)-quad core GT ₄ +OPC	—	TBD	67		
		S(35W)-dual core GT ₂	—	TBD	36		
		S(65W)-dual core GT ₂	—	TBD	36		
		S(35W)-quad core GT _{2/0}	—	TBD	66		
		S(65W)-quad core GT _{2/0}	—	TBD	79		
I _{CTDC}	Thermal Design Current (TDC) for processor IA Cores Rail	—	—	—	Refer to the appropriate Processor Platform Power Architecture Guide (see related documents)	A	9
		—	—	—	—	—	—
TOB _{VCC}	Voltage Tolerance	PS0, PS1	—	—	±20	mV	3,6,8
		PS2, PS3	—	—	±20	mV	3,6,8
Ripple	Ripple Tolerance	—	—	—	I _L ≤ 0.5	mV	3,6,8
		PS0	—	—	0.5 < I _L < I _{CTDC}		
		PS1	—	—	I _{CTDC} < I _L < I _{CCMAX}		
		PS2	—	—	—		
DC _{LL}	Loadline slope within the VR regulation loop capability	Y-processor line	—	4.7	5.9	mΩ	10,13
		U-dual core GT ₂	—	—	2.4		
		U-dual core GT ₃ +OPC	—	—	2.4		
		H-quad core GT ₂	—	—	1.8		
		H-quad core GT ₄ +OPC	—	—	1.6		
AC _{LL}	AC Loadline	Y/U/H/S	—	—	Max DC _{LL} (up to 400KHz)	mΩ	10,13
		Y-processor line	—	—	18.3(LL1, range: 29±1.5MHz)		

+VCC_CORE [42]
+VCCSTG [6]
+VCCSTPLL [2,4,6,9,41,42]



Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
V _{DDQ} (DDR3L/-RS)	Processor I/O supply voltage for DDR3L/-RS	All	—	1.35	—	V	3,4,5
V _{DDQ} (LPDDR3)	Processor I/O supply voltage for LPDDR3	All	—	1.20	—	V	3,4,5
V _{DDQ} (DDR4/-RS)	Processor I/O supply voltage for DDR4/-RS	All	—	1.20	—	V	3,4,5
TOB _{VDDQ}	VDDQ Tolerance	All	DC: ±2 AC: ±3 AC+DC: ± 5			%	3,4
I _{CCMAX_VDDQ} (DDR3L/-RS)	Max Current for V _{DDQ} Rail (DDR3L/-RS)	U S	—	—	2	A	2
I _{CCMAX_VDDQ} (LPDDR3)	Max Current for V _{DDQ} Rail (LPDDR3)	Y H	—	—	2	A	2
I _{CCMAX_VDDQ} (DDR4/-RS)	Max Current for V _{DDQ} Rail (DDR4/-RS)	H	—	—	2.8	A	2

Symbol	Parameter	Segment	Min	Typ	Max	Units	Notes 1
VCC _{ST}	Processor Vcc Sustain supply voltage	All	—	1.0	—	V	3
TOB _{ST}	VCC _{ST} Tolerance	All	AC+DC:± 50			mV	3
ICC _{MAX_ST}	Max Current for VCC _{ST}	Y	—	—	100	mA	4
		U			120		
		H			120		
		S			120		

Table 7-13. Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications (Sheet 1)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes ^{1,2}
TOB _{CCPLL}	V _{CCPLL} Tolerance	All	AC+DC; ± 50			mV	3
I _{CCMAX_VCCPLL}	Max Current for V _{CCPLL} Rail	Y	—	—	100	mA	
		U	—	—	120		
		H	—	—	145		
		S	—	—	130		

Symbol	Parameter	Segment	Min	Typ.	Max	Unit	Note ^{1,2}
V _{CCIO}	Voltage for the memory controller and shared cache	Y U,H,S		0.85 0.95	—	V	3
TOB _{VCCIO}	V _{CCIO} Tolerance	All	AC+DC: ± 50			mV	3
I _{CCMAX_VCCIO}	Max Current for V _{CCIO} Rail	Y U H S	— — — —	— — — —	3 3.1 5.5 5.5	A	

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note ^{1,2}
V _{CCSA}	Voltage for the System Agent	Y-processor line	0.55	—	1.05	V	3,5
		U-processor line	0.55	—	1.15		
		H-processor line	0.55	—	1.15		
		S-processor line (fixed voltage)	—	1.05	—		
TOB _{VCCSA}	V _{CCSA} Tolerance	Y/U/H-processor lines S-processor line	±20 ±50(DC+AC+ripple)			mV	3
I _{CCMAX_VC} CSA	Max Current for V _{CCSA} Rail	Y-processor line	—	—	4.1	A	
		U-dual core GT2	—	—	4.5		
		U-dual core GT3+OPC	—	—	5.1		
		H-quad core GT2	—	—	11.1		
		H-quad core GT4+OPC	—	—	8		
		S-processor line	—	—	11.1		
DC_LL	V _{CCSA} Loadline	Y-processor line	—	14	18	mΩ	6,7
		U-dual core GT2	—	—	10.3		
		U-dual core GT3+OPC	—	—	10.3		
		H-quad core GT2	—	—	10		
		H-quad core GT4+OPC	—	—	6		
		Y/U/H/S	—	—	Max DC_LL (up to 400KHz) 43.2(LL1, range: 12.3±1.5MHz) 42.6(LL2, range: 2±1.5MHz)		
AC_LL	AC Loadline	Y-processor line	—	—		mΩ	6,7

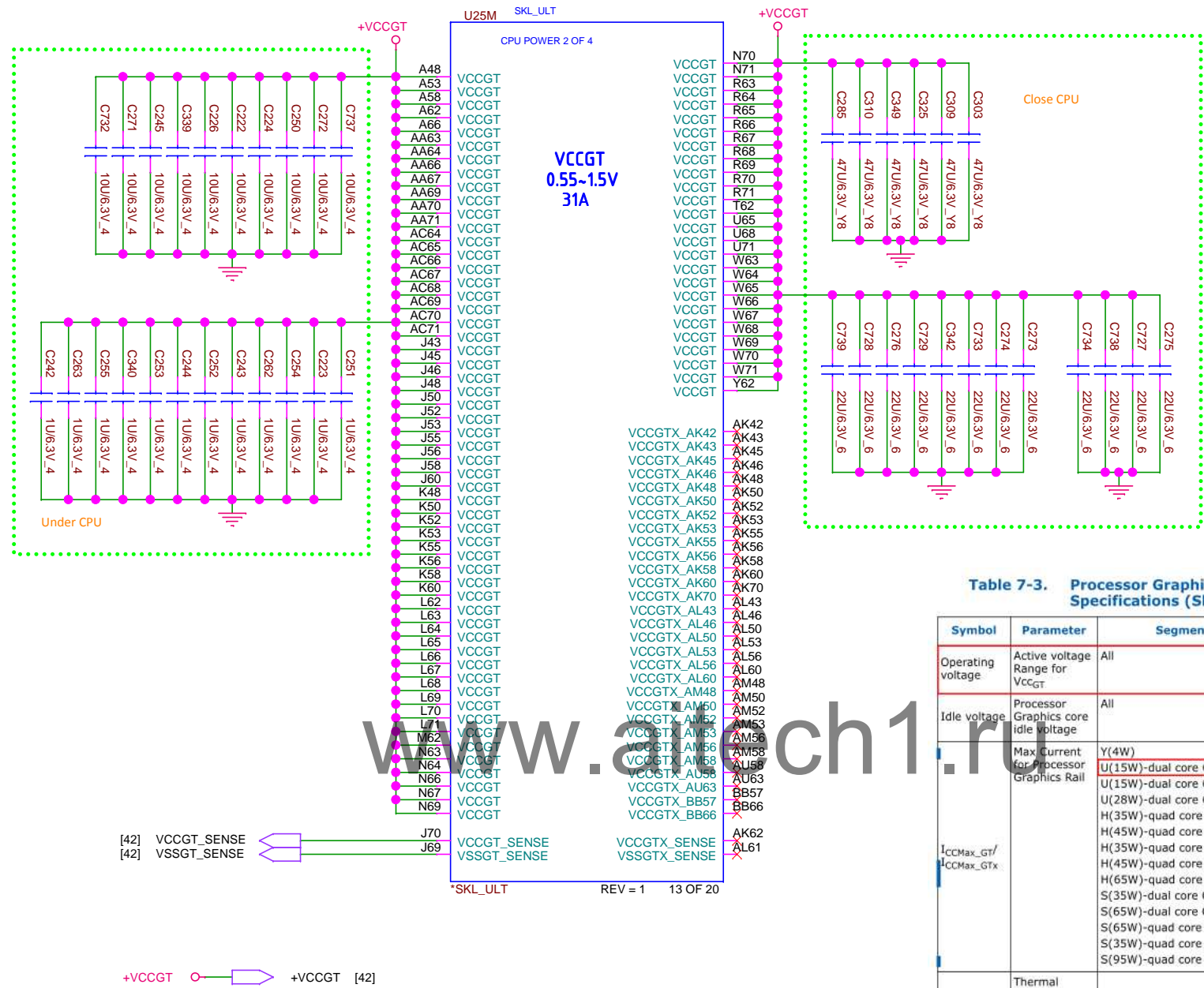
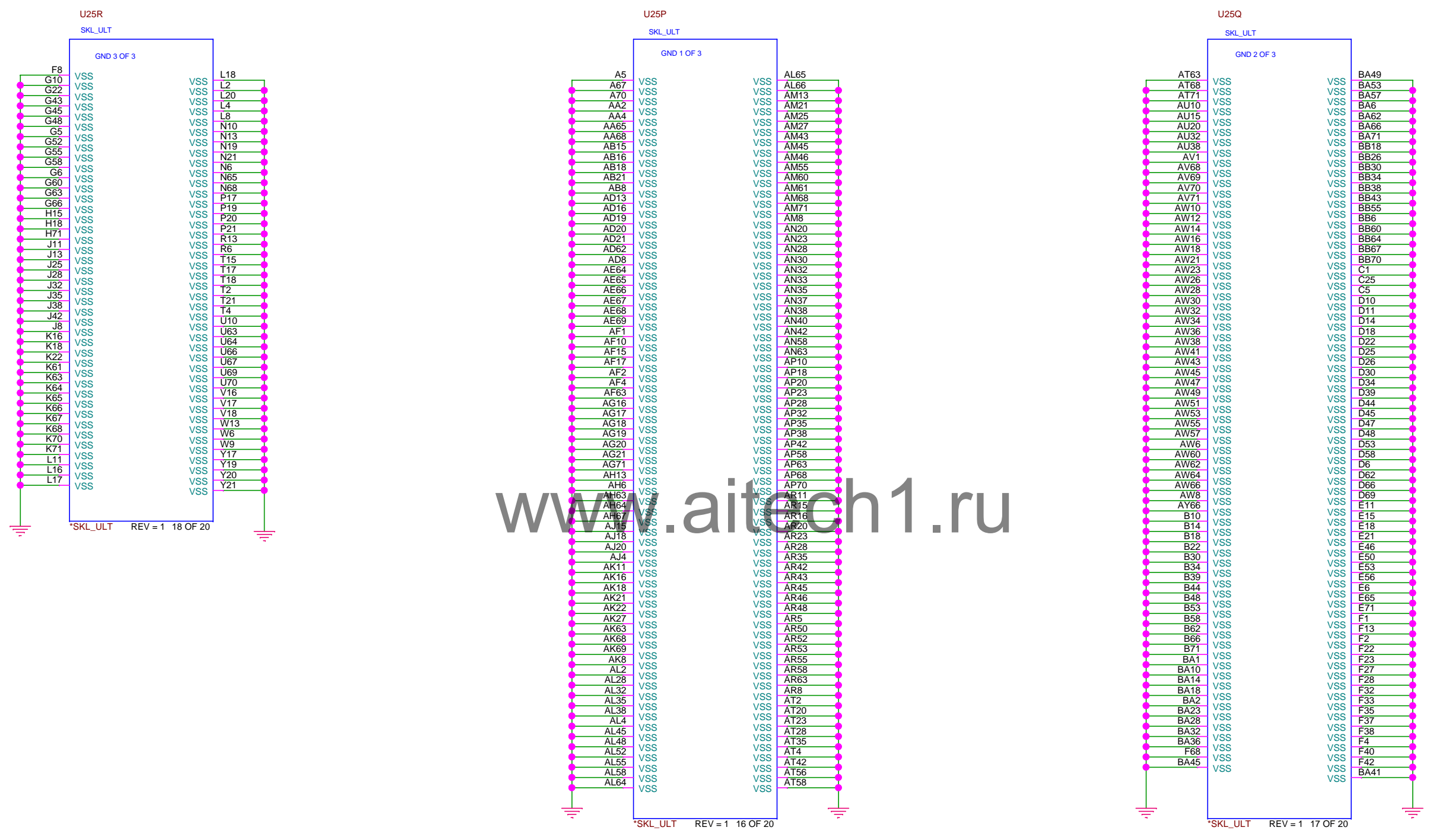
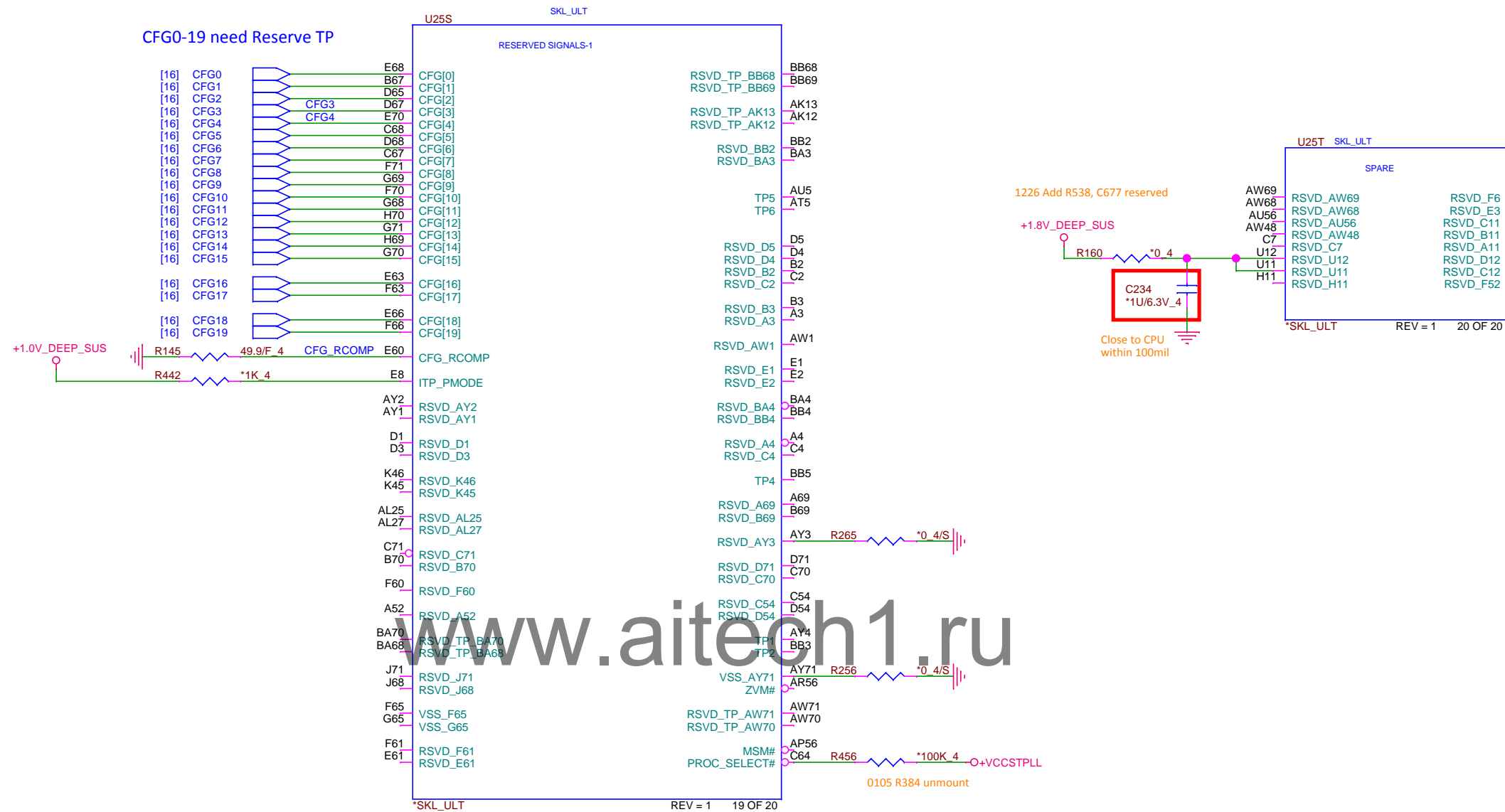


Table 7-3. Processor Graphics (Vcc_{GT} and Vcc_{GT-X}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

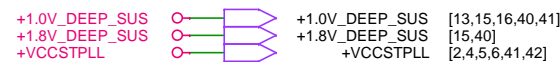
Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note ¹
Operating voltage	Active voltage Range for Vcc _{GT}	All	0.55	—	1.5	V	2,3,6,8
Idle voltage	Processor Graphics core idle voltage	All	0	—	0.55	V	3
I _{CCMax_GT} /I _{CCMax_GTX}	Max Current for Processor Graphics Rail	Y(4W)	—	—	24		
		U(15W)-dual core GT2	—	—	31		
		U(15W)-dual core GT3+OPC	—	—	57/7(GTx)		
		U(28W)-dual core GT3+OPC	—	—	57/7(GTx)		
		H(35W)-quad core GT2	—	—	55		
		H(45W)-quad core GT2	—	—	55		
		H(35W)-quad core GT4+OPC	—	—	94/9(GTx)		
		H(45W)-quad core GT4+OPC	—	—	94/12(GTx)		
		H(65W)-quad core GT4+OPC	—	—	94/14(GTx)		
		S(35W)-dual core GT2	—	—	48		
		S(65W)-dual core GT2	—	—	48		
		S(65W)-quad core GT2	—	—	51		
		S(35W)-quad core GT2	—	—	46		
		S(95W)-quad core GT2	—	—	51		
I _{CCTDC_GT}	Thermal Design Current (TDC) for Processor Graphics Rail	—	—	—	Refer to the appropriate Processor Platform Power Architecture Guide (see related documents)		A 6
TOB _{GT}	Vcc _{GT} Tolerance	PS0,PS1	—	—	±20	mV	3,4
		PS2,PS3	—	—	±20	mV	3,4
Ripple	Ripple Tolerance	—	—	—	I _L <= 0.5 0.5 < I _L < I _{CCTDC} I _{CCTDC} < I _L < I _{CCMax}		
		PS0	—	—	+30/-10 ±10 ±15	mV	3,4
		PS1	—	—	+30/-10 ±15 ±15	mV	3,4
		PS2	—	—	+30/-10 +30/-10 +30/-10	mV	3,4
		PS3	—	—	+30/-10 +30/-10 +30/-10	mV	3,4
DC_LL	Vcc _{GT} Loadline slope	Y-processor line	—	4.2	5.7		
		U-dual core GT2	—	—	3.1		
		U-dual core GT3+OPC	—	—	2/6.0(GTx)		
		H-quad core GT2	—	—	2.65	mΩ	7,9
		H-quad core GT4+OPC	—	—	1.4/6.0(GTx)		
AC_LL	AC Loadline	Y/U/H/S	—	—	Max DC_LL (up to 400KHz) 3.9(LL1, range: 25±1.5MHz) 12.1(LL2, range: 4±1.5MHz)	mΩ	7,9
		Y-processor line	—	—			

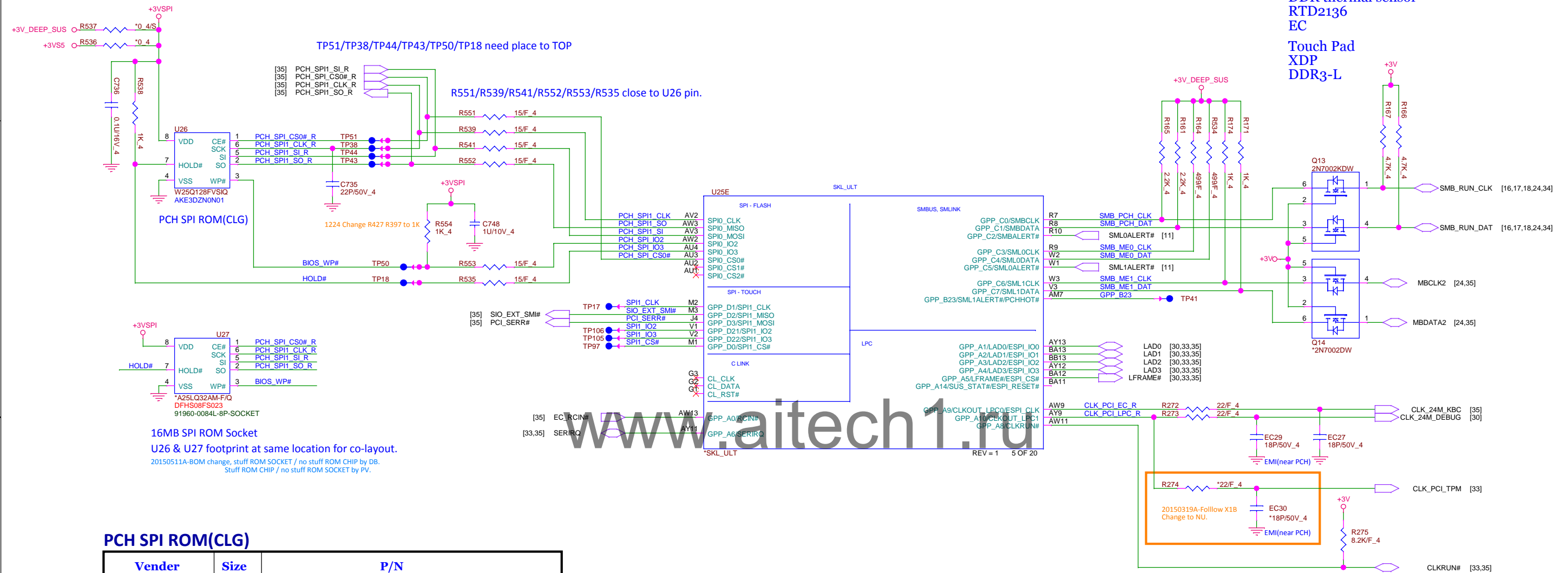




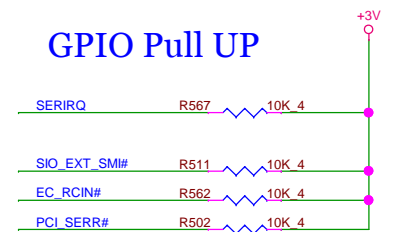
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	



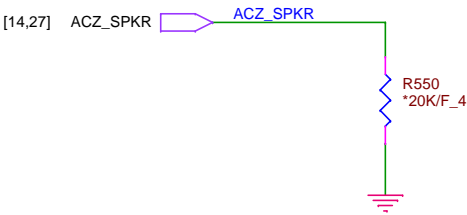


GPIO Pull UP

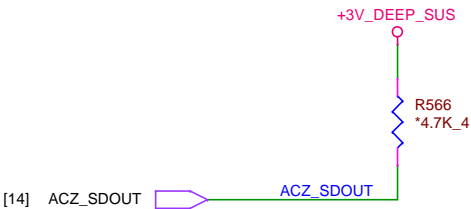


Functional Strap Definitions

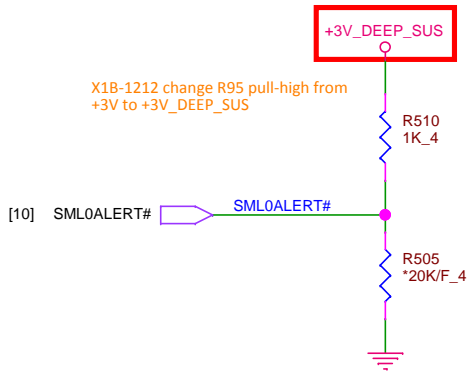
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



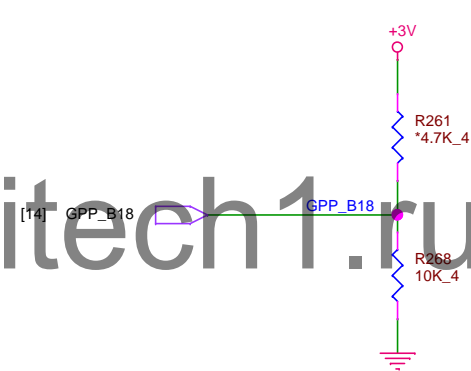
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



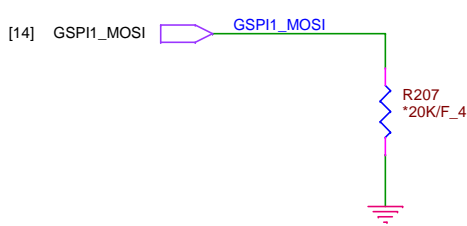
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



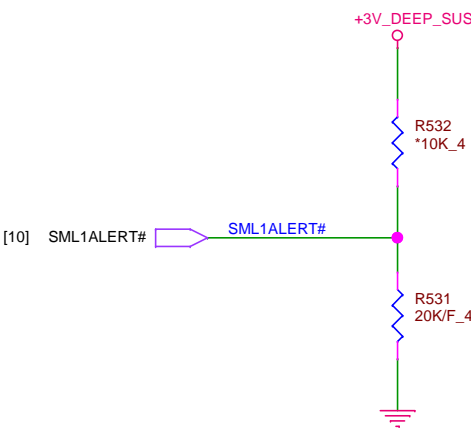
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



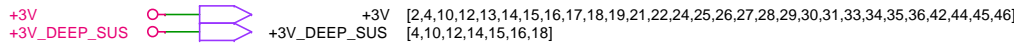
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



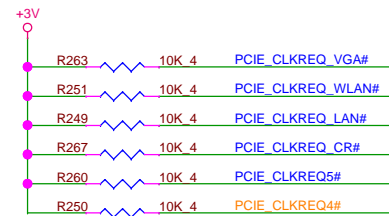
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.



CLK_REQ/Strap Pin(CLG)



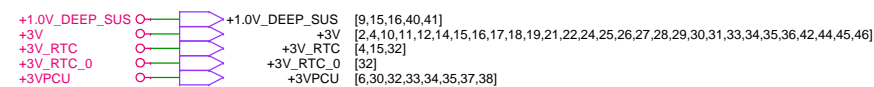
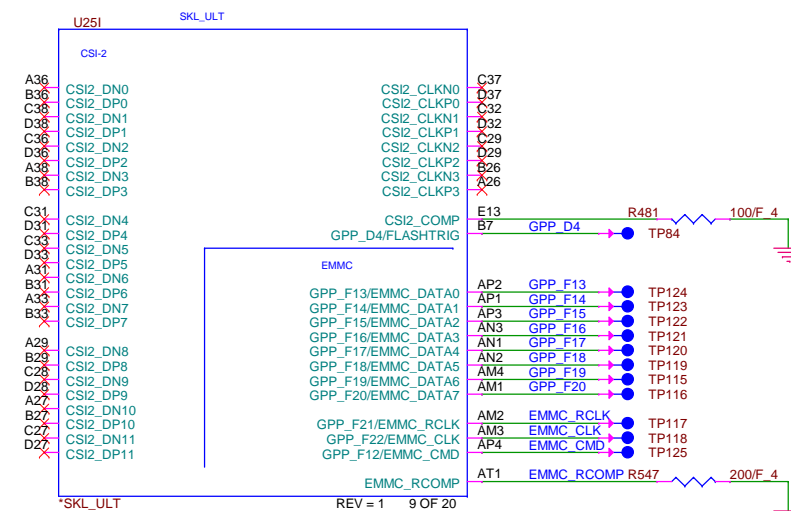
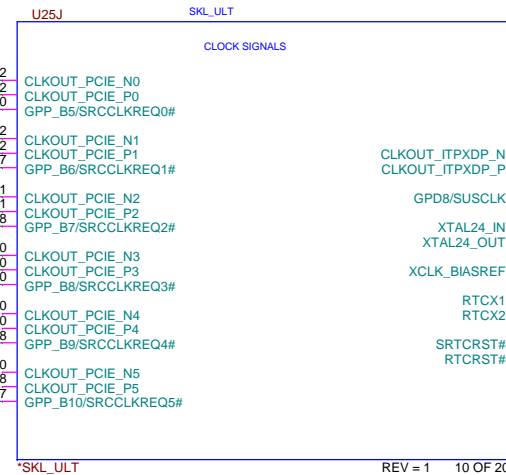
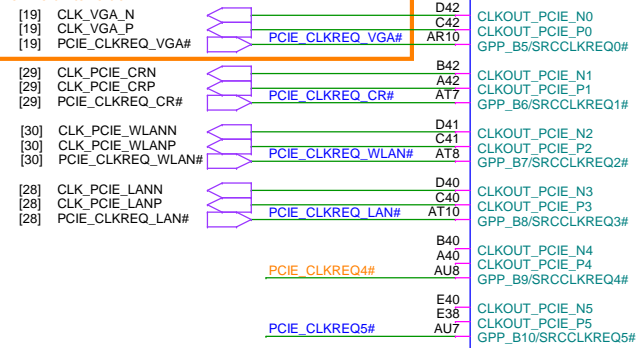
20150319A-Follow X18
Change VGA CLK from Port-4 to Port-0.

VGA

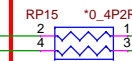
Card Reader

WLAN

LAN

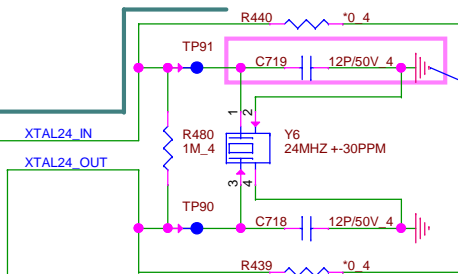


RP3 install for XDP



PCH_SUSCLK [31] 20150312A-ADD

20150713A3-PV-R
20150727A1-PV-R change for crystal.



20150601A-Change C719 to NU. R440 change from 0Ω to 22Ω for terminal resistor.

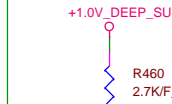
20150525A-BOM change to same with DB stage.

20150518A-XTAL24_IN from G-CLK. Screen has flicker when all CPU workload on 100%. Root-cause is PCH_XTAL24_IN too close +VCC_CORE. Vender recommend to add CAP 10pF on C719.

External Crystal and Green Clock

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

20150319A-Follow X18 change to 10pF CAP.

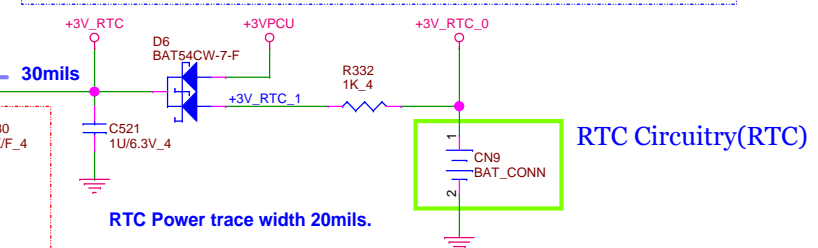


RTC Clock 32.768KHz

20150518A-Change RTC 32.768KHz from G-CLK since PV stage.

20150520A-Change C744, C745 to 10pF base on EPSON test result.

+3V_RTC
 Pass by Diode = 3.079V
 Pass by G-CLK = 2.712V
 +3V_RTC_0
 3.206V
 3.135V
 +3V_RTC can't pass by G-CLK IC because G-CLK has more ΔV.



RTC Circuitry(RTC)

RTC Power trace width 20mils.

1223 change J1 to R524 unmount Function for RESET.

EC_RTC_RST:
 Watch Dog for system can't boot and need remove RTC battery & clear CMOS.

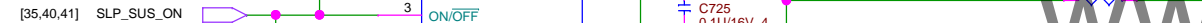



Quanta Computer Inc.

PROJECT : TWL & JWL (MB)

Size	Document Number	Rev.
C	SKL-12 (CLK/eMMC)	3C
Date:	Wednesday, July 29, 2015	Sheet : 13 of 51

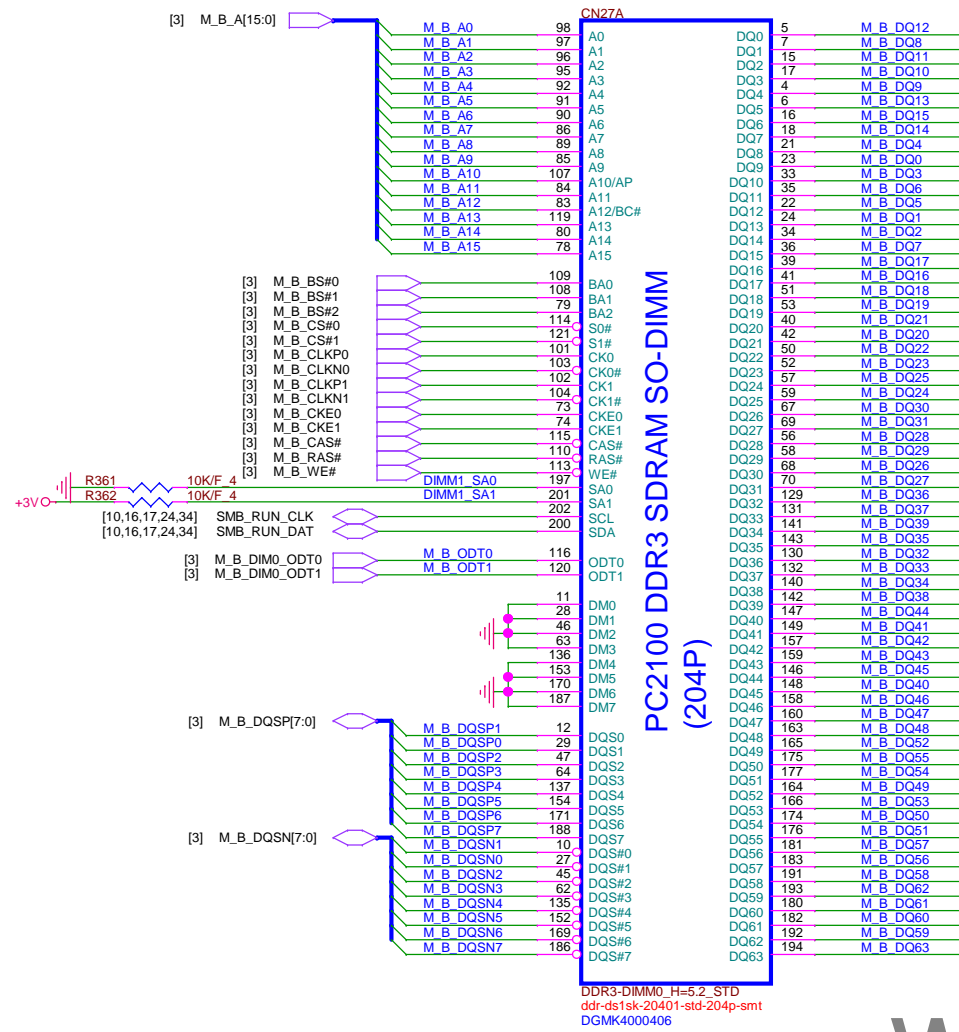




 Quanta Computer Inc. PROJECT : TWL & JWL (MB)		
Size C	Document Number SKL-14 (PCH POWER)	Rev. 3C
Date:	Wednesday, July 29, 2015	Sheet : 15 of 51

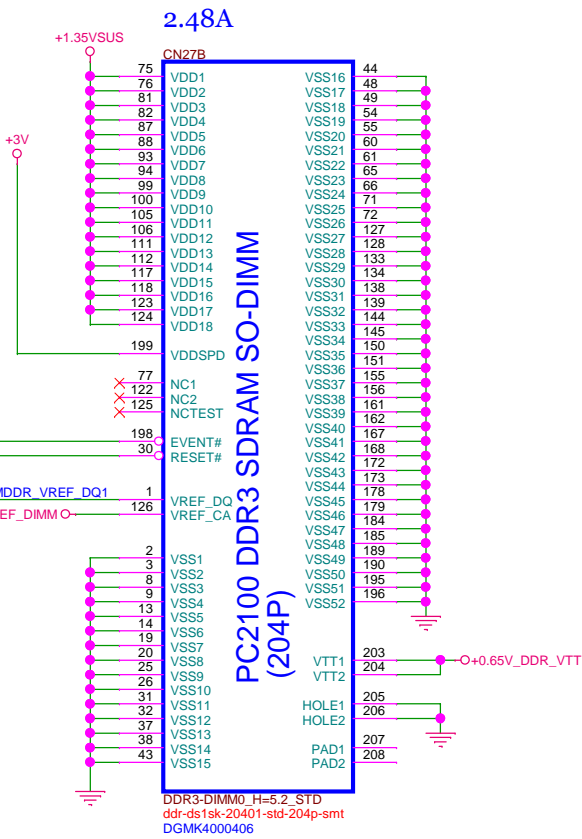
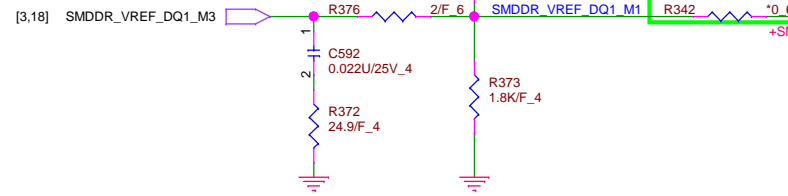






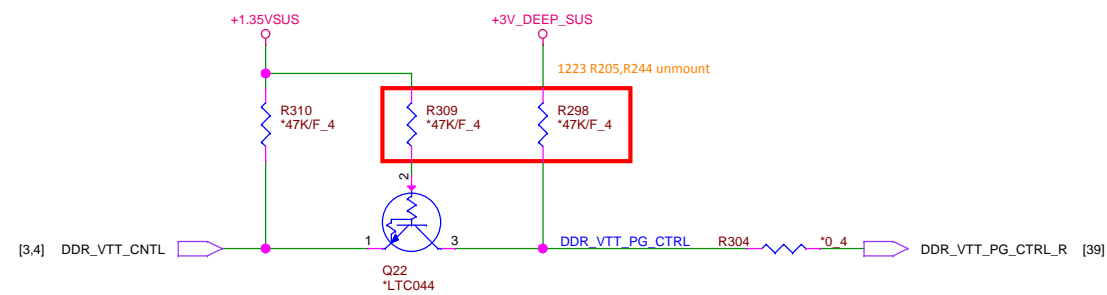
M_B_DQ[63:0] [3]

VREF DQ1 M1 Solution

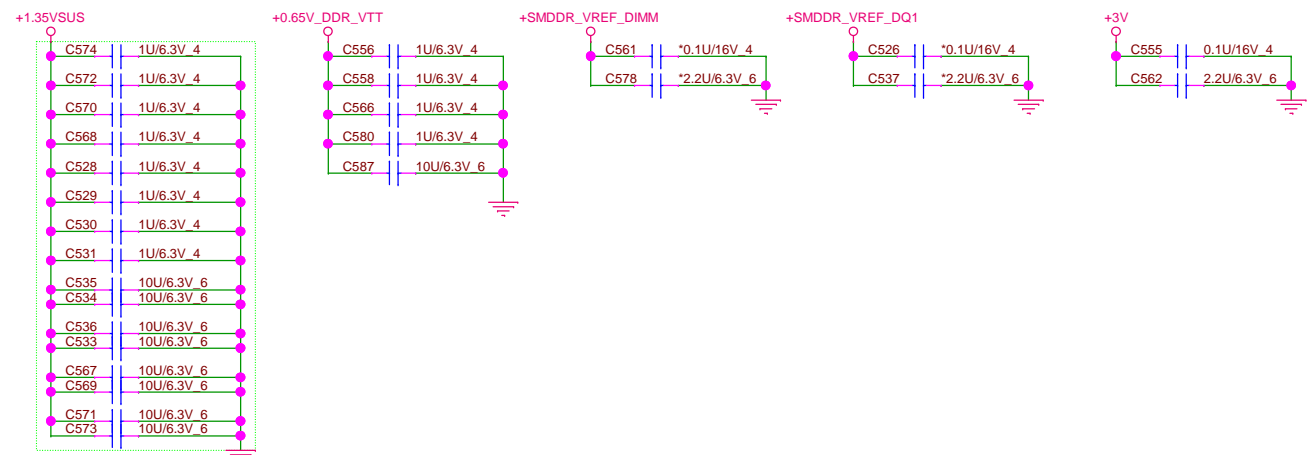


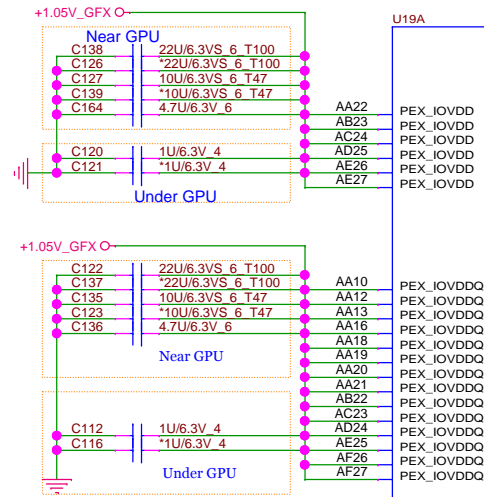
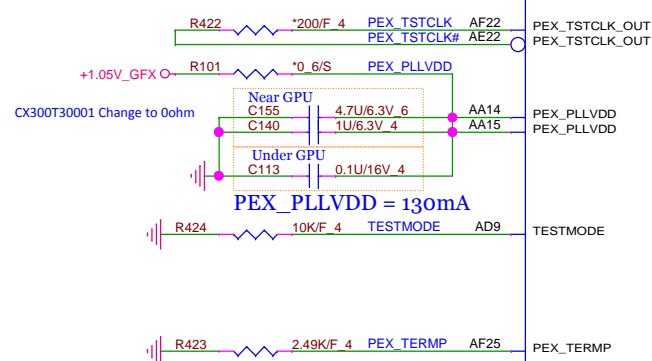
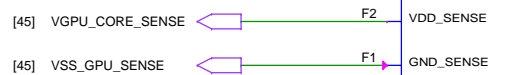
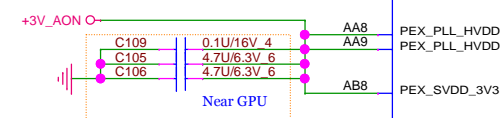
www.aitech1.ru

Co-lay for ODT
From Intel MOW, ODT directly connection to CPU

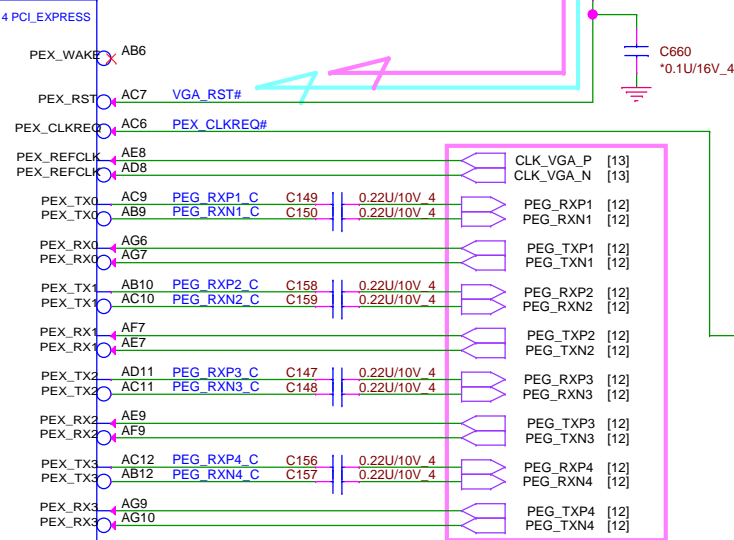
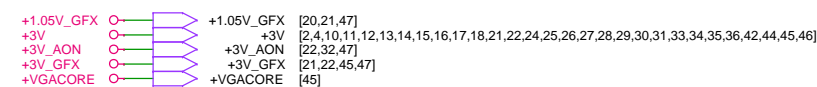
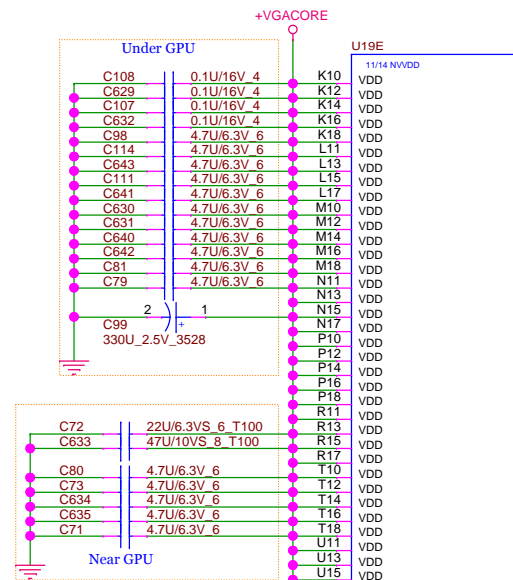


Place these CAPS near SO-DIMM-1.
1uF/10uF 4pcs on each side of connector

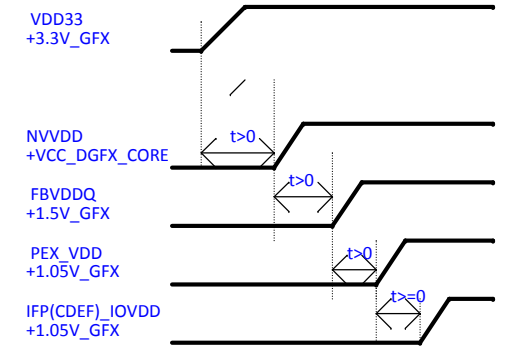


$$\text{PEX_IOVDD} + \text{PEX_IOVDDQ} = 1.042\text{A}$$

$$\text{PEX_PLL_HVDD} + \text{PEX_SVDD_3V3} = 143\text{mA}$$


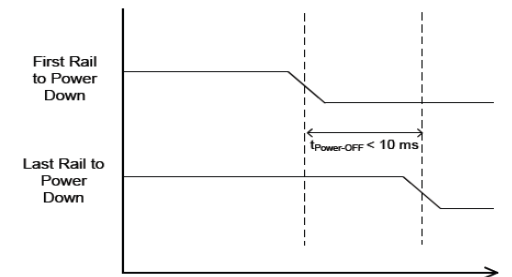
N16V-GM not support GC6 function


$$NVDD = 32.22 \sim 26.66 \text{ A}$$


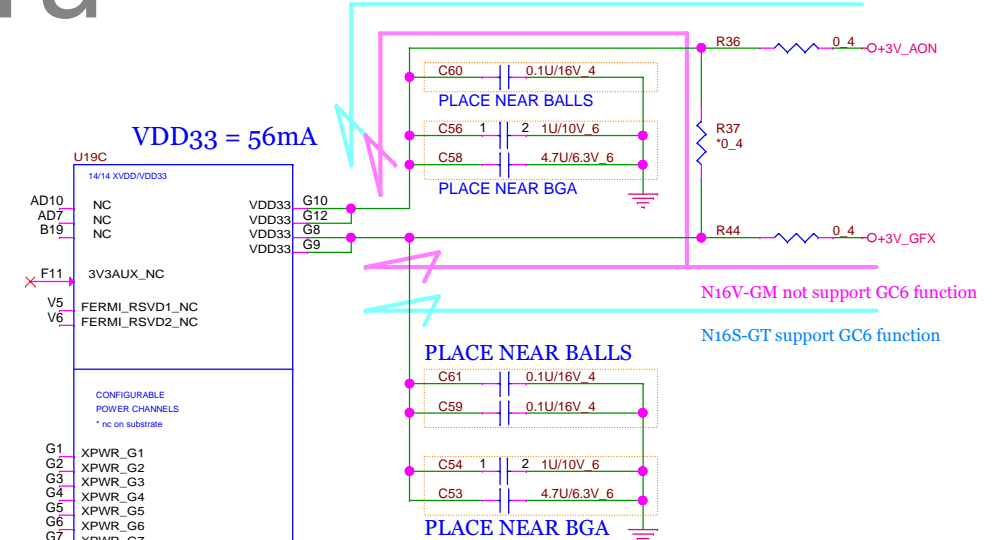
Power Up Sequence



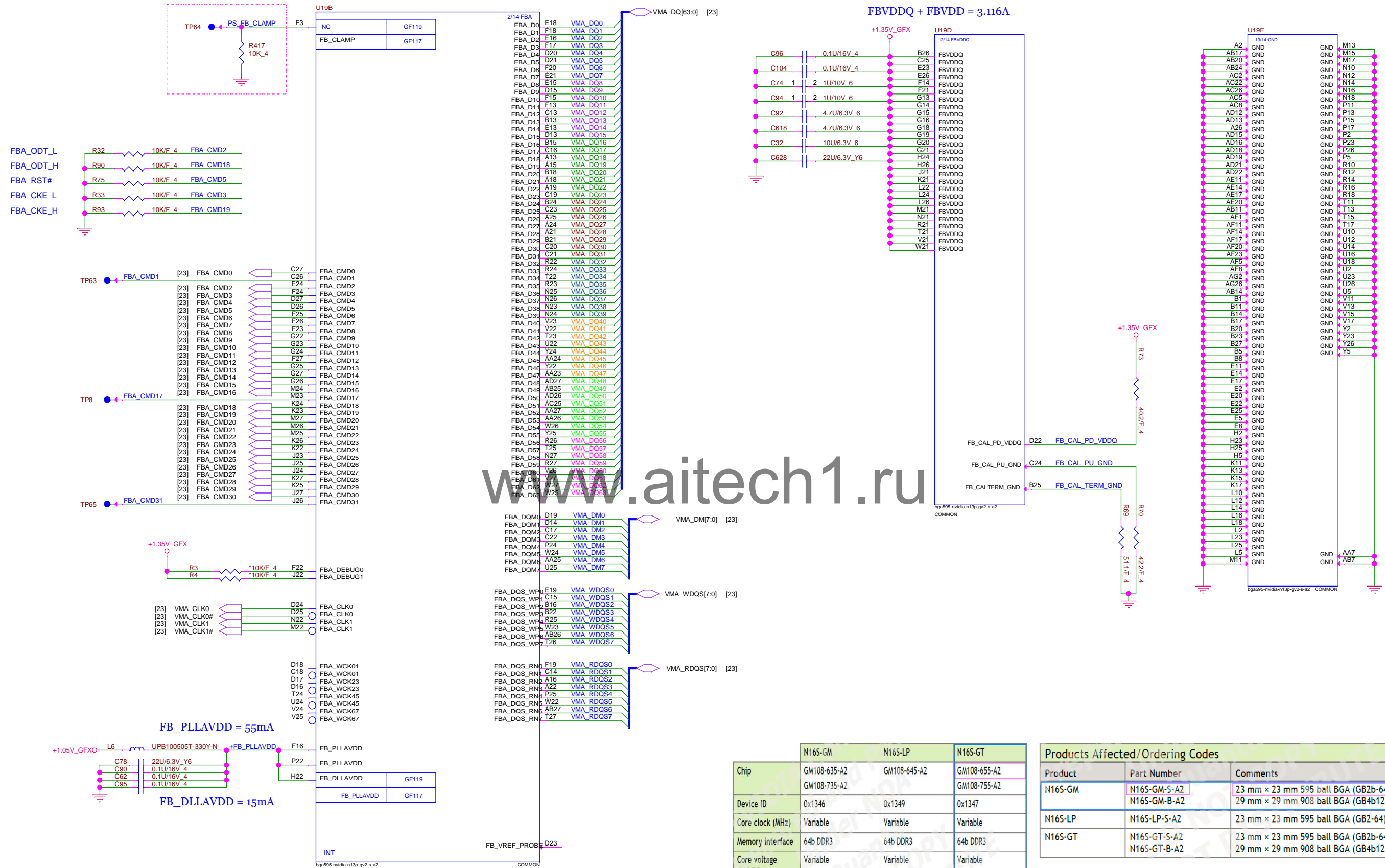
Power Down Sequence



BOM Default by N16S-GT for Support GC6 2.0.
N16S-GT support GC6 function

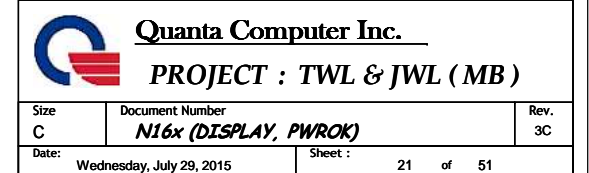


20140804A-NV recommand ball : F3 keep NC.
20140919A-NV recommand add 10KΩ PD on ball-F3 to avoid GPU entry GC6 1.0 state when floating.
Some S3/S4 long run test fail is due to ball-F3 floating.

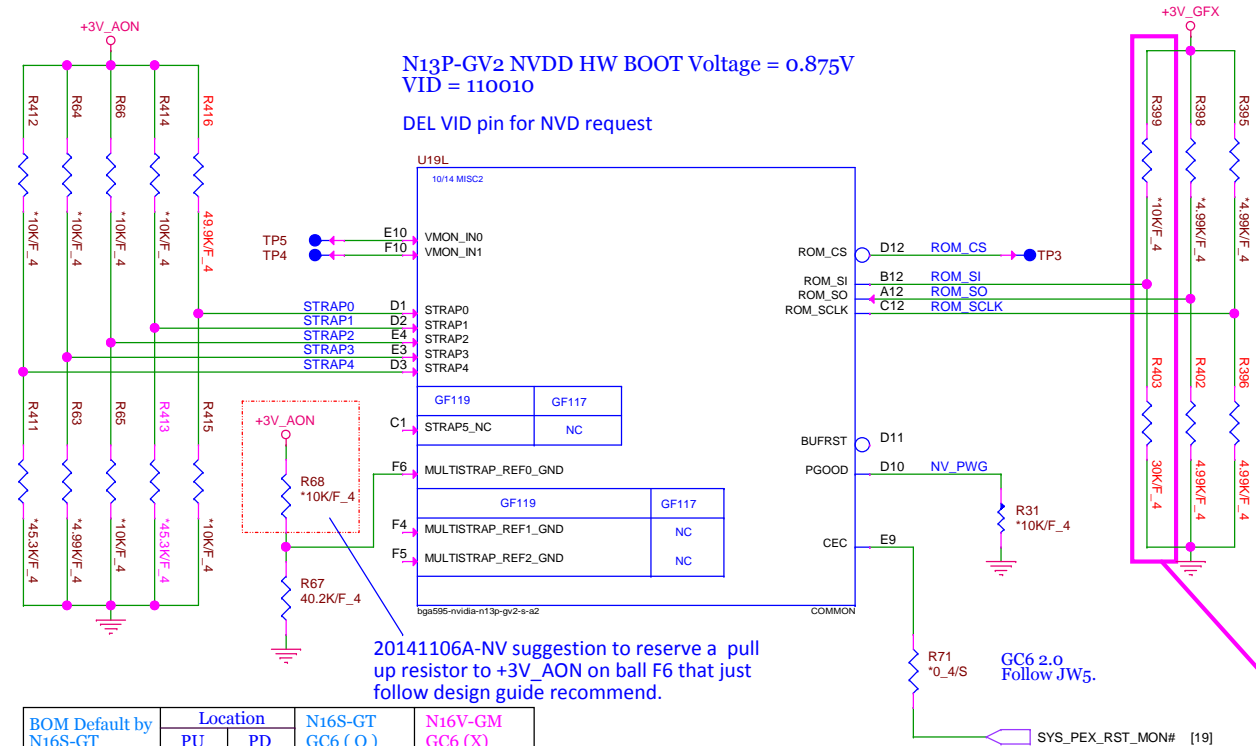
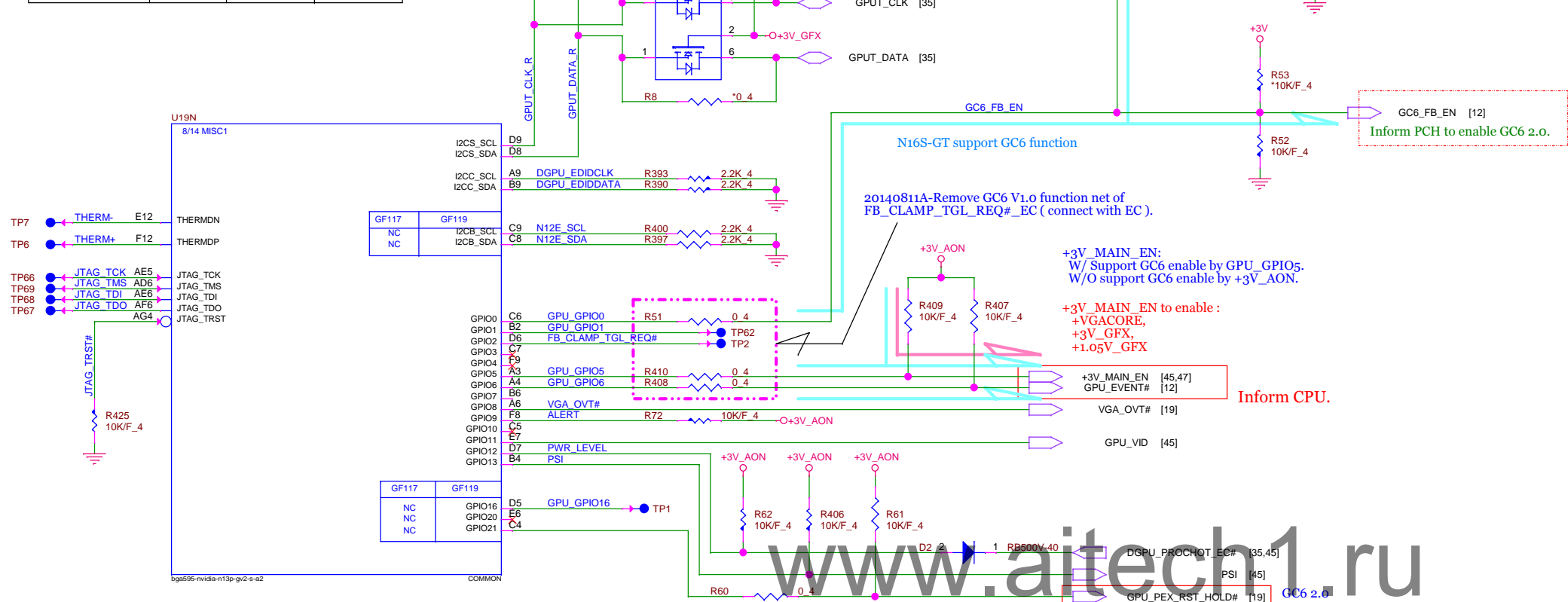


	N16S-GM	N16S-LP	N16S-GT
Chip	GM108-635-A2 GM108-735-A2	GM108-645-A2	GM108-655-A2 GM108-755-A2
Device ID	0x1346	0x1349	0x1347
Core clock (MHz)	Variable	Variable	Variable
Memory interface	64b DDR3	64b DDR3	64b DDR3
Core voltage (NVDD)	Variable	Variable	Variable
Package	GB2b-64 (23 mm × 23 mm 595 balls) GB4b-128 (29 mm × 29 mm 908 balls)	GB2b-64 (23 mm × 23 mm 595 balls)	GB2b-64 (23 mm × 23 mm 595 balls) GB4b-128 (29 mm × 29 mm 908 balls)

Products Affected/Ordering Codes		
Product	Part Number	Comments
N16S-GM	N16S-GM-S-A2	23 mm × 23 mm 595 ball BGA (GB2b-64)
	N16S-GM-B-A2	29 mm × 29 mm 908 ball BGA (GB4b128)
N16S-LP	N16S-LP-S-A2	23 mm × 23 mm 595 ball BGA (GB2-64)
N16S-GT	N16S-GT-S-A2	23 mm × 23 mm 595 ball BGA (GB2b-64)
	N16S-GT-B-A2	29 mm × 29 mm 908 ball BGA (GB4b128)



BOM Default by N16S-GT		N16S-GT GC6 (O)	N16V-GM GC6 (X)
GPU_GPIO0	R51	STUFF	NO STUFF
GPU_GPIO5	R410 R409	STUFF STUFF	NO STUFF STUFF
GPU_GPIO6	R408 R407	STUFF STUFF	NO STUFF STUFF



ROM_SI (Memory strap setting)

BOM Default by 30.1KΩ PD for Samsung K4W4G1646D-BC1A for N16S-GT.

Quanta P/N	VRAM	Part Description	Value	Resistor
AKD5PGWTW05	Hynix	H5TC4G63AFR-11C	0*3 0011	PD 20.0KΩ (R403)
AKD5PGWT500	Samsung	K4W4G1646D-BC1A	0*5 0101	PD 30.1KΩ (R403)
AKD5PZDTW00	Hynix	H5TC4G63CFR-NoC	0*2 0010	PD 15.0KΩ (R403)
AKD5MZDTW04	Hynix	H5TC2G63FFR-11C	0*9 1001	PU 10.0KΩ (R399)
AKD5MGST511	Samsung	K4W2G1646Q-BC1A	0*B 1011	PU 20.0KΩ (R399)

Quanta P/N	VRAM	Part Description	Value	Resistor
AKD5PGWTW05	Hynix	H5TC4G63AFR-11C	0*E 1110	PU 34.8KΩ (R399)
AKD5PGWT500	Samsung	K4W4G1646D-BC1A	0*5 0101	PD 30.1KΩ (R403)
AKD5MZDTW04	Hynix	H5TC2G63FFR-11C	0*B 1011	PU 20.0KΩ (R399)
AKD5MGST511	Samsung	K4W2G1646Q-BC1A	0*7 0111	PD 45.3KΩ (R403)
AKD5PZDTW00	Hynix	H5TC4G63CFR-NoC	0*0 0000	PD 4.99KΩ (R403)

BOM Default by N16S-GT	Location	PU	PD	N16S-GT GC6 (O)	N16V-GM GC6 (X)
ROM_SI	R399	R403	RVL	RVL	RVL
ROM_SO	R398	R402	PD 4.99KΩ	PU 4.99KΩ	PU 4.99KΩ
ROM_SCLK	R395	R396	PD 4.99KΩ	PU 4.99KΩ	PU 4.99KΩ
STRAP0	R416	R415	PU 49.9KΩ	PU 45.3KΩ	PU 45.3KΩ
STRAP1	R414	R413	NU	PD 45.3KΩ	PD 45.3KΩ
STRAP2	R66	R65	NU	PU 10KΩ	PU 10KΩ
STRAP3	R64	R63	NU	PD 4.99KΩ	PD 4.99KΩ
STRAP4	R412	R411	NU	PD 45.3KΩ	PD 45.3KΩ

+3V_AON [2,4,10,11,12,13,14,15,16,17,18,19,21,24,25,26,27,28,29,30,31,33,34,35,36,42,44,45,46]
+3V_GFX [19,21,45,47]

ROM_SI (Memory strap setting)

* Both for 940M (N16S-GT) & 920M (N16V-GM)

Following J7WU VRAM:

VRAM P/N	VRAM	Vender	VRAM Size
AKD5PGWTW05	IC SDRAM(96P)H5TC4G63AFR-11C(FBGA)	Hynix	4G*4=16G=2G bytes
AKD5PGWT500	IC SDRAM(96P)K4W4G1646D-BC1A(FBGA)	Samsung	4G*4=16G=2G bytes

Hynix new VRAM C-die P/N: AKD5PZDTW00 IC SDRAM(96P)H5TC4G63CFR-NOC(FBGA)

* Both for 940M (N16S-GT) & 920M (N16V-GM)

VRAM P/N	VRAM	VRAM Size
AKD5MZDTW04	Hynix IC SDRAM(96P)H5TC2G63FFR-11C(FBGA)	2G*4pcs=1G bytes
AKD5MGST511	Samsung IC SDRAM(96P)K4W2G1646Q-BC1A(FBGA)	2G*4pcs=1G bytes

Table 15-2. Resistance Mapping to Hex Values

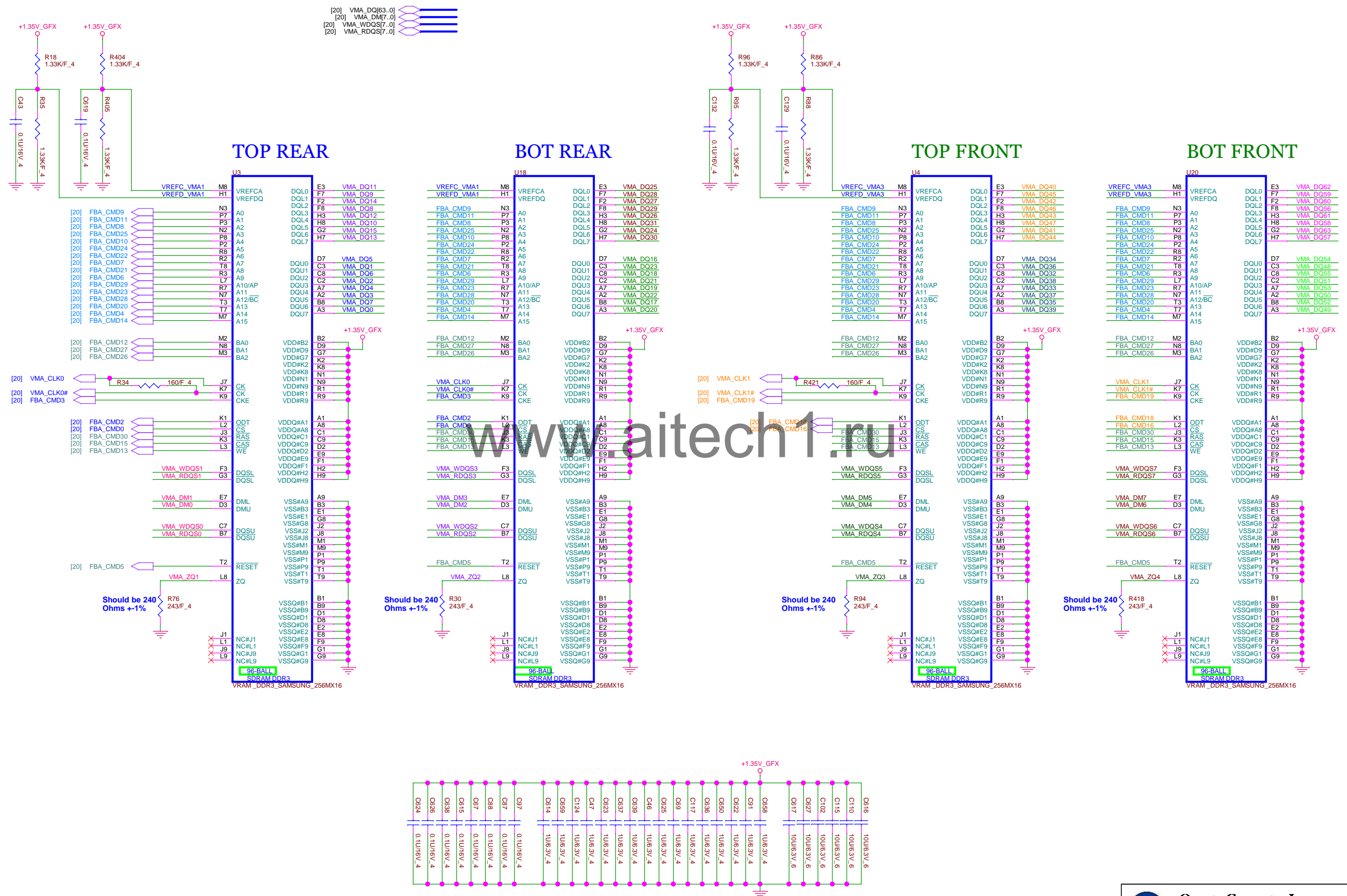
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001 Ox1 Micron
15.0 kΩ	1010	0010 Ox2 Hynix
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100 Ox4 Samsung
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 4. N16S-GM/-GT/-LP DDR3L Recommended Memories

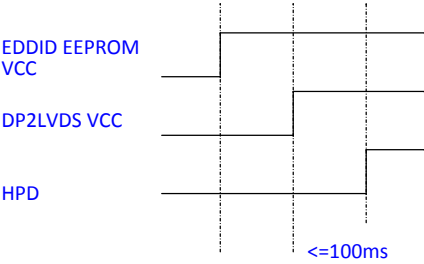
Memory Type	FBVDD/FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	1001	Production ready
				Micron	MT41J128M16JT-093G-K	K-die	0xA	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0x8	900	1011	Production ready
				Hynix	H5TC4G63AFR-11C	A-die	0x3	900	0011	Production ready
				Micron	MT41J256M16HA-093G-E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	0101	Production ready
	1.35V/1.35V	256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Samsung	K4W4G1646E-BC1A	E-die	0x1	900	N/A	Post production ready
				Hynix	H5TC4G63CFR-11C	C-die	0x2	900	0010	Production ready
				Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G-E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0xF	900	N/A	Post production ready

Table 2. N16V-GM DDR3L Recommended Memories

Memory Type	FBVDD/FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x8	900	1011	Production ready
				Micron	MT41J128M16JT-093G-K	K-die	0x8	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0x7	900	0111	Production ready
				Hynix	H5TC4G63AFR-11C	A-die	0xE	900	1110	Production ready
				Micron	MT41J256M16HA-093G-E	E-die	0x0	900	N/A	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	0101	Production ready
	1.35V/1.35V	256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Samsung	K4W4G1646E-BC1A	E-die	0x2	900	N/A	Post production ready
				Hynix	H5TC4G63CFR-11C	C-die	0x0	900	0000	Production ready
				Hynix	H5TC4G63AFR-11C	A-die	0xE	900	N/A	Production ready
				Micron	MT41J256M16HA-093G-E	E-die	0xD	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0xC	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x0	900	N/A	Post production ready



RTD2136S Power Up Sequence



AUX Channel : 6inch/85Ω

Main Link : 6inch/85Ω

5.1 Power On/Off Sequence

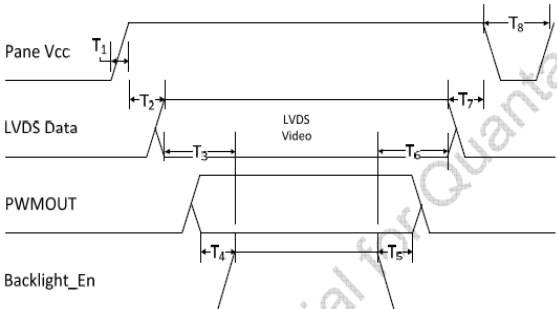


Figure 5-1 Panel On/off Sequence

Table 5-1 Timing parameters of Power On/Off Sequence

Time Para.	Description	Min.(ms)	Max.(ms)
T ₁	Rising time of Panel Vcc	0.5	10
T ₂	Delay from Panel Vcc output enable to LVDS output enable	0	50
T ₃	Delay from LVDS output enable to backlight output enable	200	--
T ₄	Delay from PWM output enable to backlight output enable	0	--
T ₅	Delay from backlight output disable to PWM out disable	0	--
T ₆	Delay from backlight output disable to LVDS output disable	200	--
T ₇	Delay from LVDS output disable to Panel Vcc output disable	0	50
T ₈	Delay between two power on/off sequence	500	--

SWR MODE	LDO MODE
Stuff Inductance	Stuff Resister

L11: need use CV-4709MN00 for Vendor suggestion

Reserve for co layout EDP CON, EDP only please stuff

LDO mode
Pin-15: LDO output
Pin-11 & 43: VDD input
Pin-17: LDO feedback

Stuff on CPU side.

Default

Reserve

ROM Mode

PANEL_VCC: Output 1A / 80mil

LVDS (RTD2136~CNN) : 7inch/90~100Ω

PIN-20 PANEL_VCC
The switch can support any panel resolution with the maximum current consumption below 1-A, and can endure panel inrush current up to 2-A.

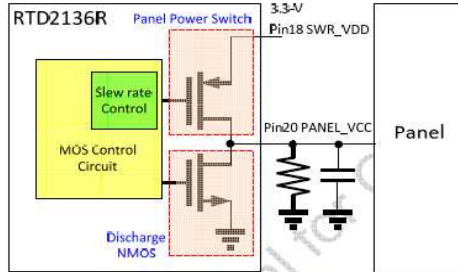


Figure 4 The application of Panel Power Switch

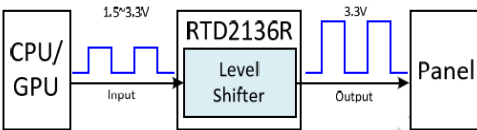
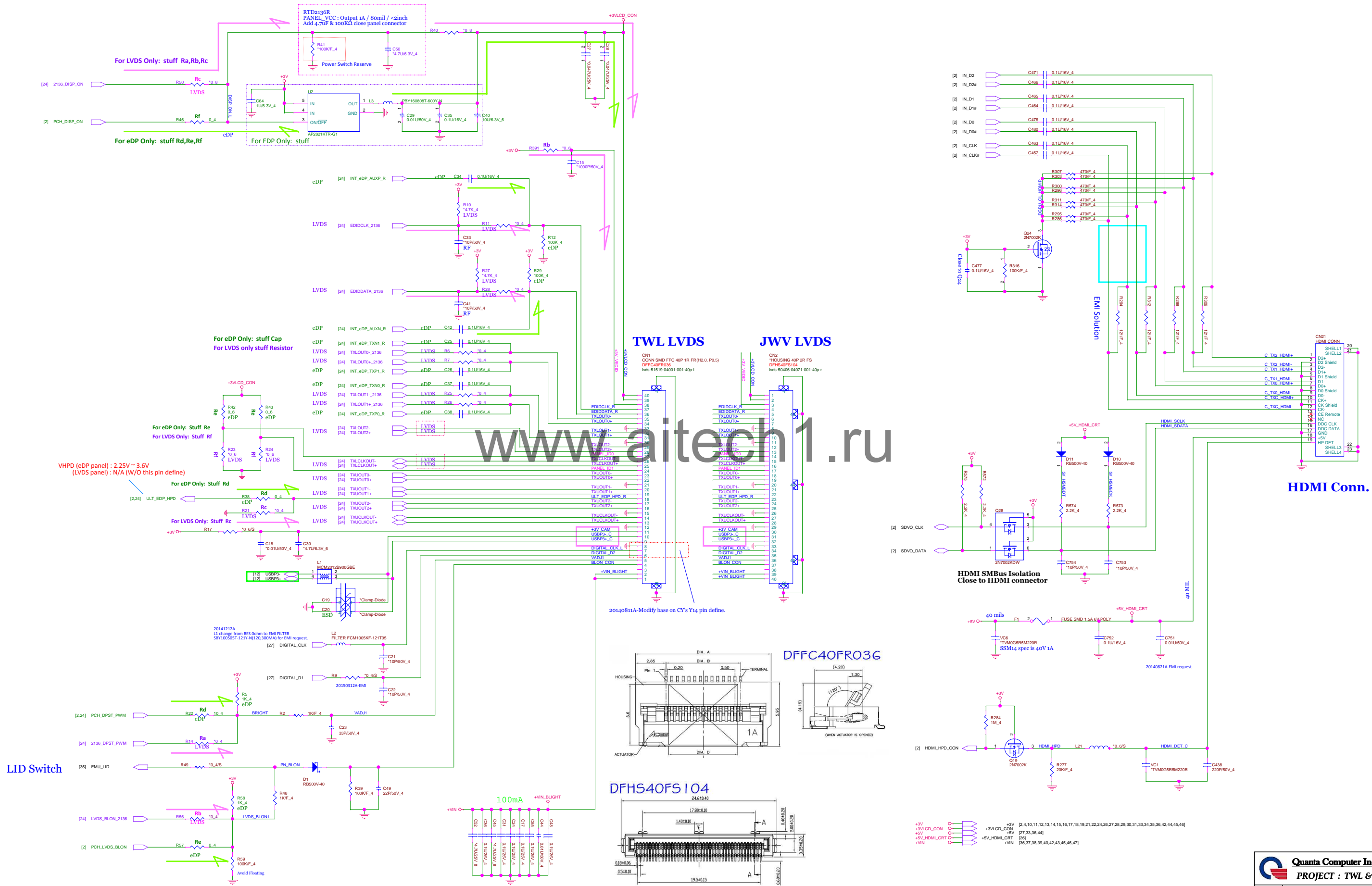
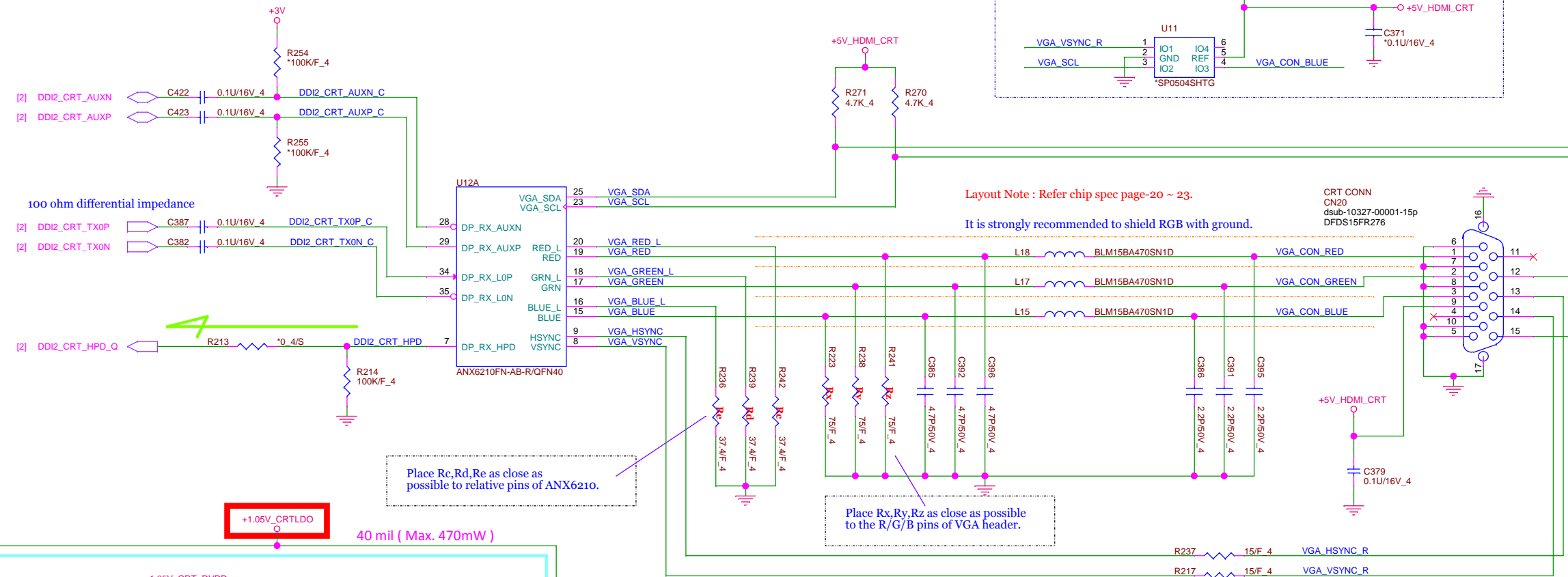
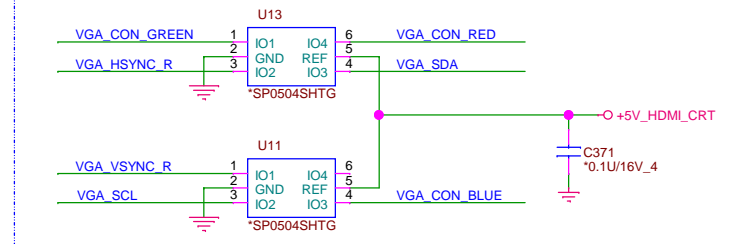


Table 5 Level Shifter Specification

Parameter	Symbol	Min	TYP	MAX	UNITS
Input High Voltage	V _{IH}	1.25	1.5	3.6	V
Input Low Voltage	V _{IL}	--	--	0.8	V
Operation Frequency	F _{PM}	--	--	3	MHz



ESD PROTECTION



Layout Note : Refer chip spec page-20 ~ 23.

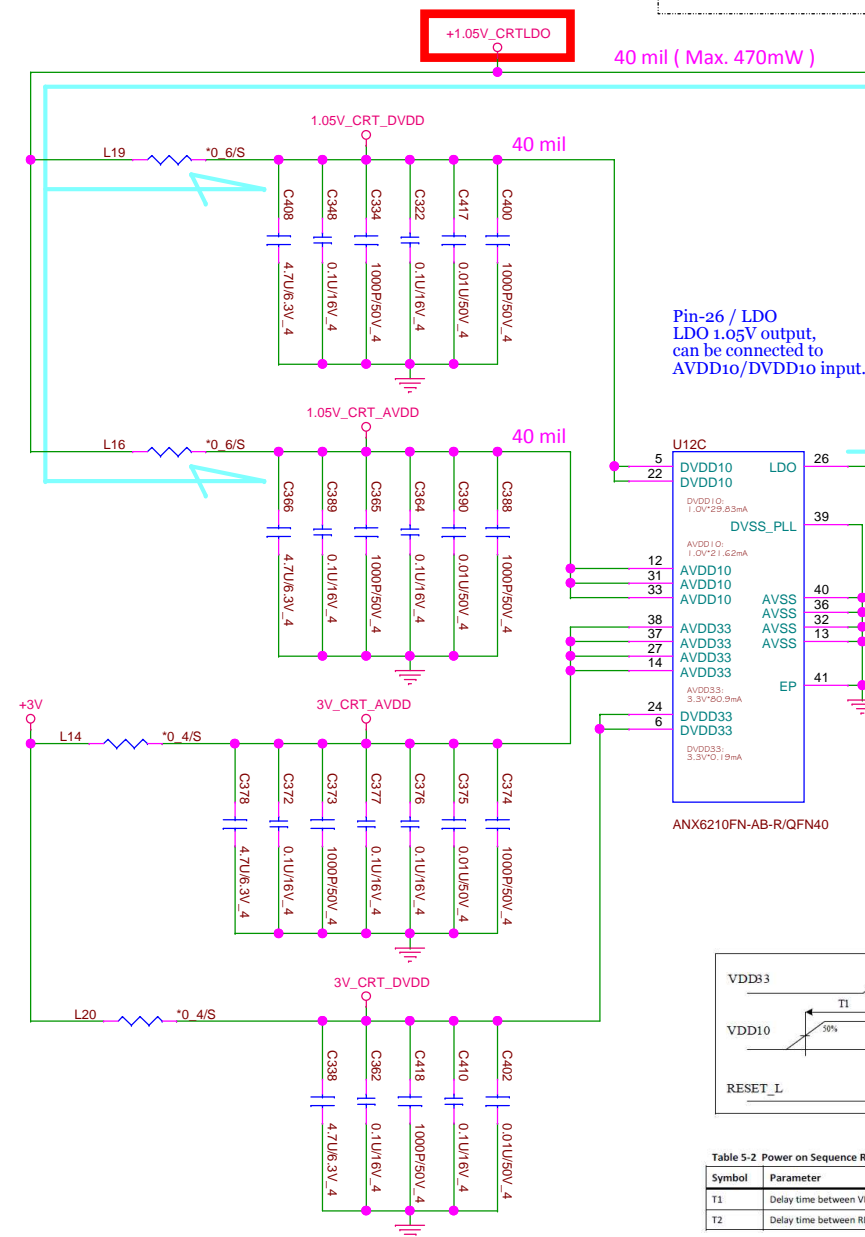
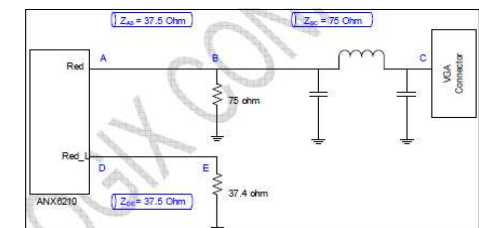
It is strongly recommended to shield RGB with ground.

CRT CONN
CN20
dsup-10327-00001-15p
DFDS15FR276

Place Rc,Rd,Re as close as possible to relative pins of ANX6210.

Place Rx,Ry,Rz as close as possible to the R/G/B pins of VGA header.

Route the VGA_RED, VEA_BLUE, VGA_GREEN, VGA_CON_RED, VGA_CON_BLUE, VGA_CON_GREEN by 75 Ohm impedance.

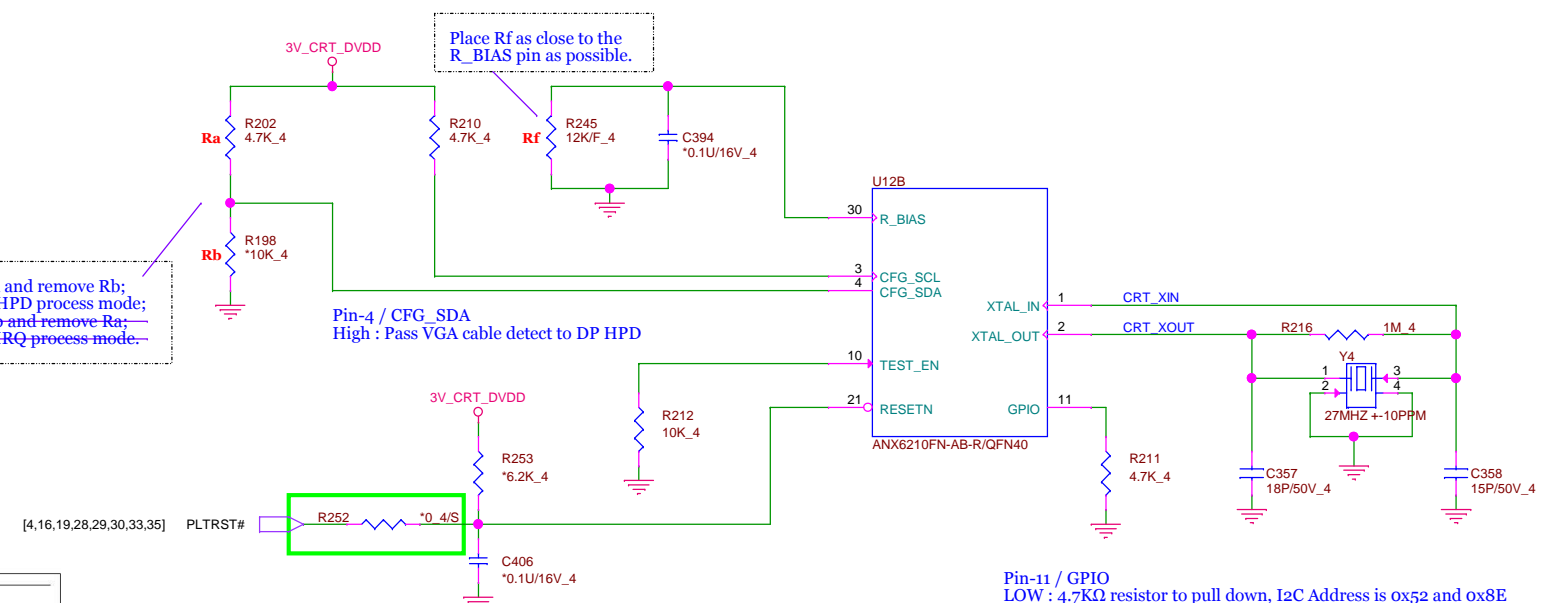


Pin-26 / LDO
LDO 1.05V output,
can be connected to
AVDD10/DVDD10 input.

Place Rf as close to the R_BIAS pin as possible.

Case 1: Keep Ra and remove Rb;
ANX6210 in HPD process mode;
Case 2: Keep Rb and remove Ra;
ANX6210 in IRQ process mode.

Pin-4 / CFG_SDA
High : Pass VGA cable detect to DP HPD



Pin-11 / GPIO
LOW : 4.7K Ω resistor to pull down, I2C Address is 0x52 and 0x8E

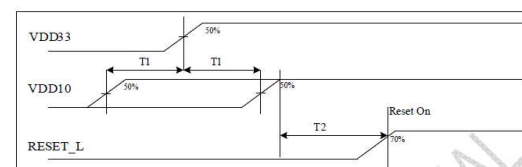
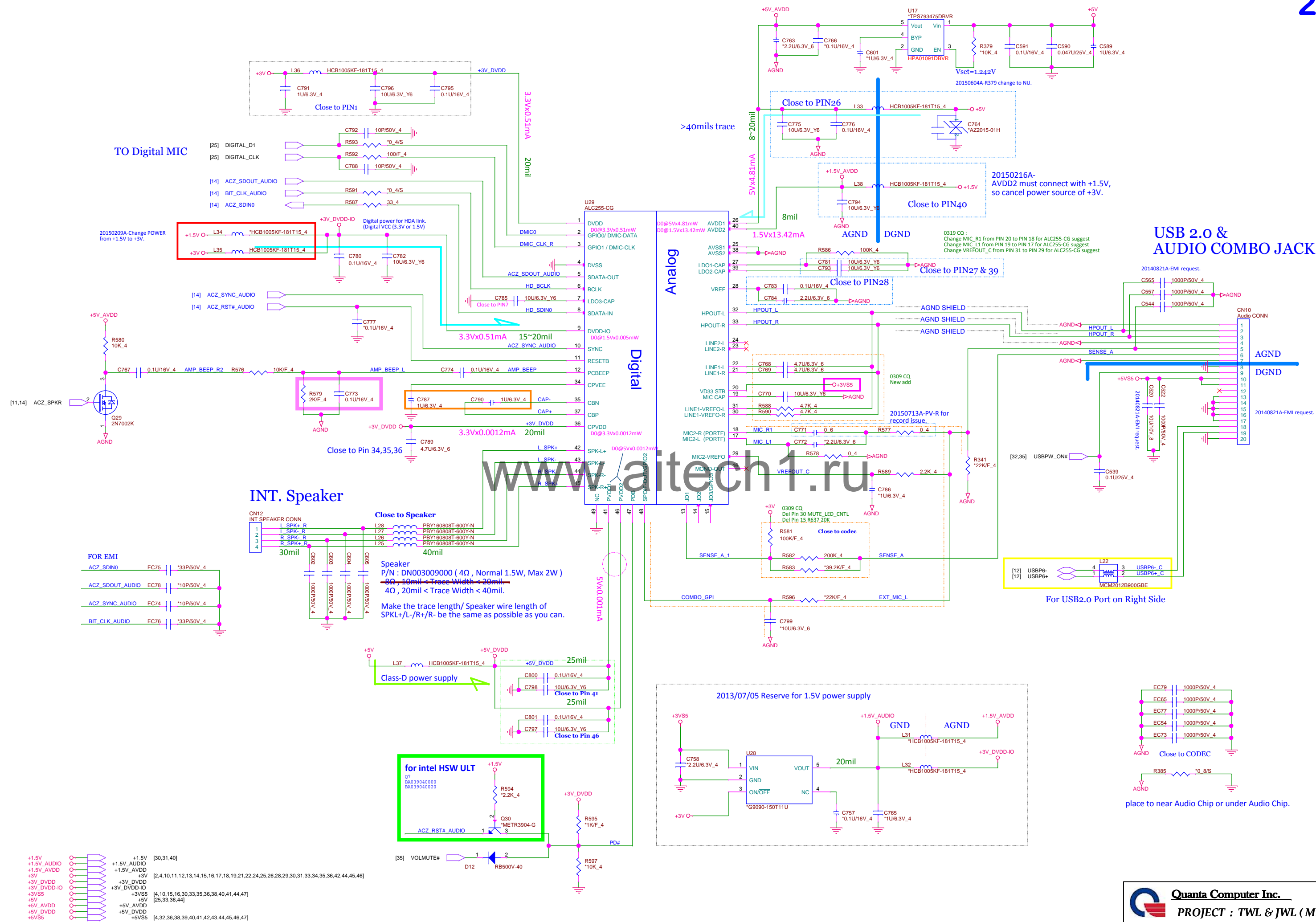


Figure 5-1 Power on Sequence

Symbol	Parameter	Min	Typ	Max	Units
T1	Delay time between VDD10 and VDD33	0	1	---	ms
T2	Delay time between RESET_L and all power rails stable	1	2	---	ms

+1.05V_CRTLDO	○	+	+1.05V_CRTLDO	
+3V	○	+	+3V	
+5V_HDMI_CRT	○	+	+5V_HDMI_CRT	[2,4,10,11,12,13,14,15,16,17,18,19,21,22,24,25,27,28,29,30,31,33,34,35,36,42,44,45,46]
1.05V_CRT_DVDD	○	+	1.05V_CRT_DVDD	
1.05V_CRT_AVDD	○	+	1.05V_CRT_AVDD	
3V_CRT_AVDD	○	+	3V_CRT_AVDD	
3V_CRT_DVDD	○	+	3V_CRT_DVDD	



9. Power Sequence

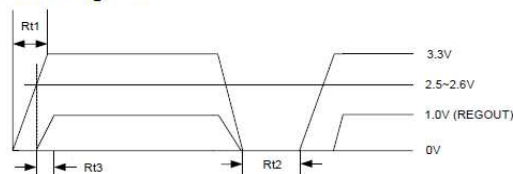


Figure 4. Power Sequence

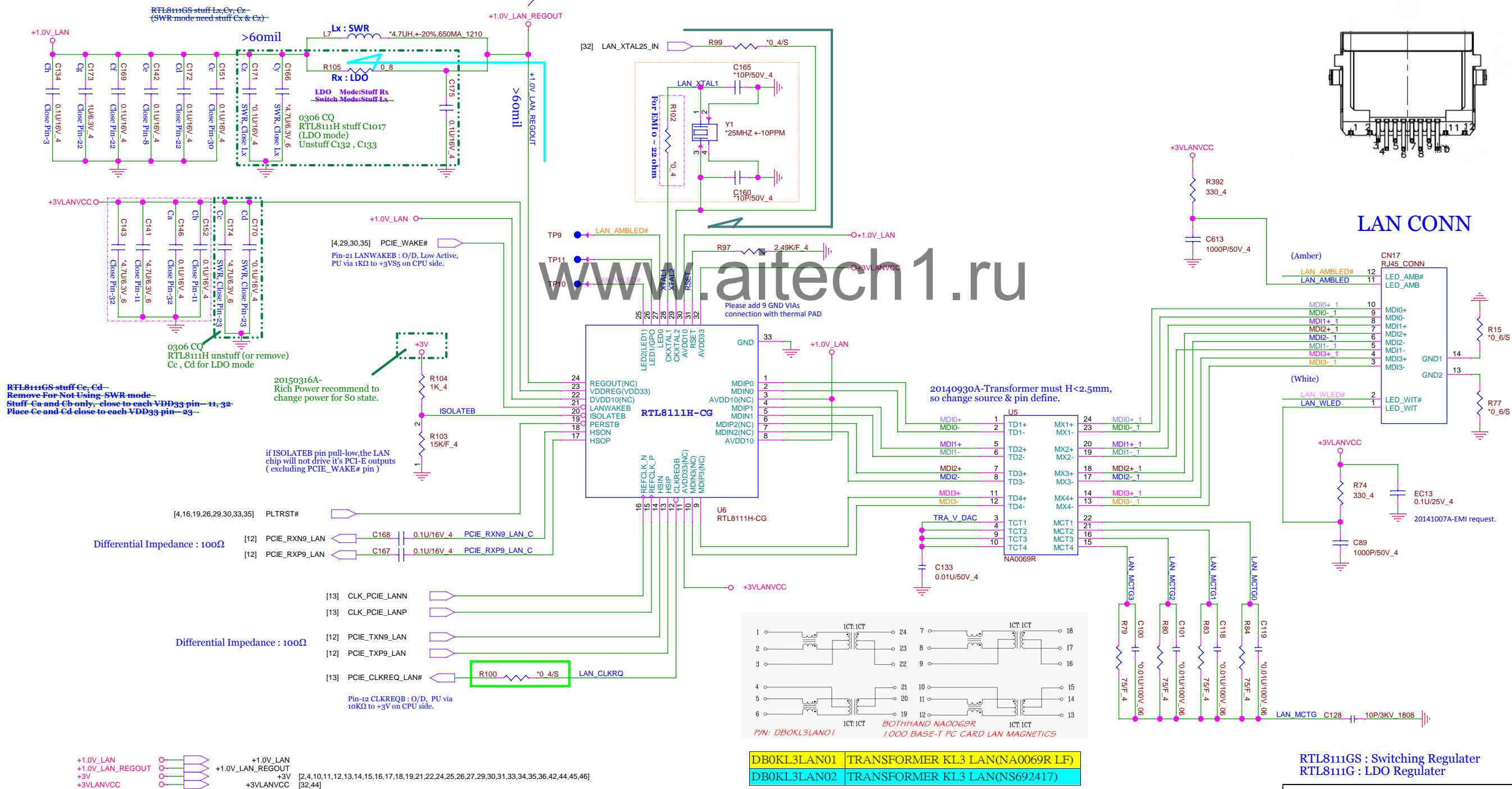
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Ch close to each VDD10 pin22

Power trace Layout W > 60mil
Trace < 30 mil
Width > 60 mil

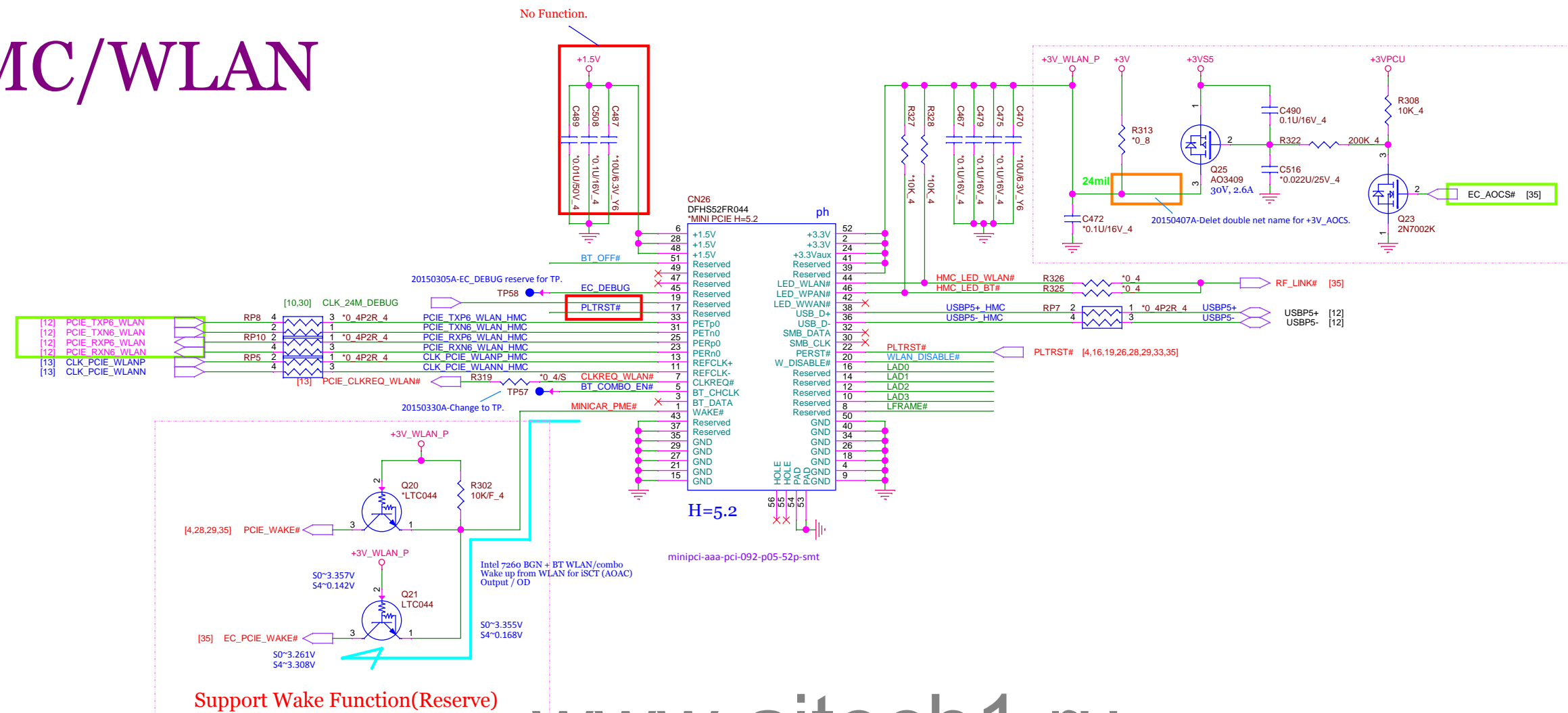
RTL8111GS (SWR Mode) Pin-24 REGOUT : Switching Regulator 1.0V Output.
RTL8111H (LDO Mode) Pin-24 REGOUT : LDO Regulator 1.0V Output.





PIN-15	SP1	SD_D1	---	I/O	SD Data 1 (SD_D1)
PIN-16	SP2	SD_Do	MS_D1	I/O	SD Data 0 (SD_Do)
PIN-17	SP3	SD_CLK	MS_Do	I/O	SD Clock signal (SD_CLK)
PIN-19	SP4	SD_CMD	MS_D2	I/O	SD CMD signal (SD_CMD)
PIN-20	SP5	SD_D3	MS_D3	I/O	SD Data 3 (SD_D3)
PIN-21	SP6	SD_D2	MS_CLK	I/O	SD Data 2 (SD_D2)
PIN-29	SP7	SD_WP	MS_BS	I	SD Write Protect signal
PIN-30	SD_CD#	SD_CD#	---	I	SD Card Detection signal

HMC/WLAN

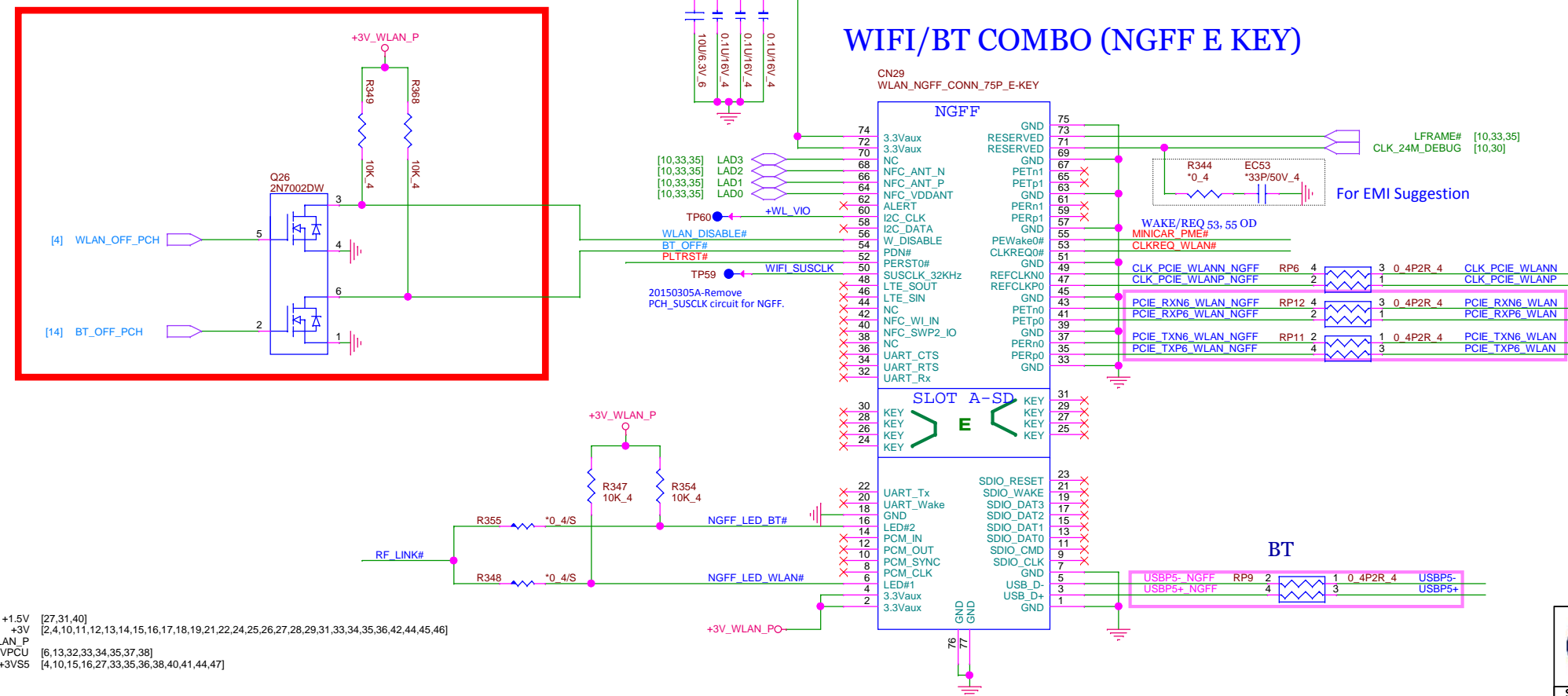


(Low Active)

WLAN_OFF_L POWER DOWN LAN CHIP from EC?

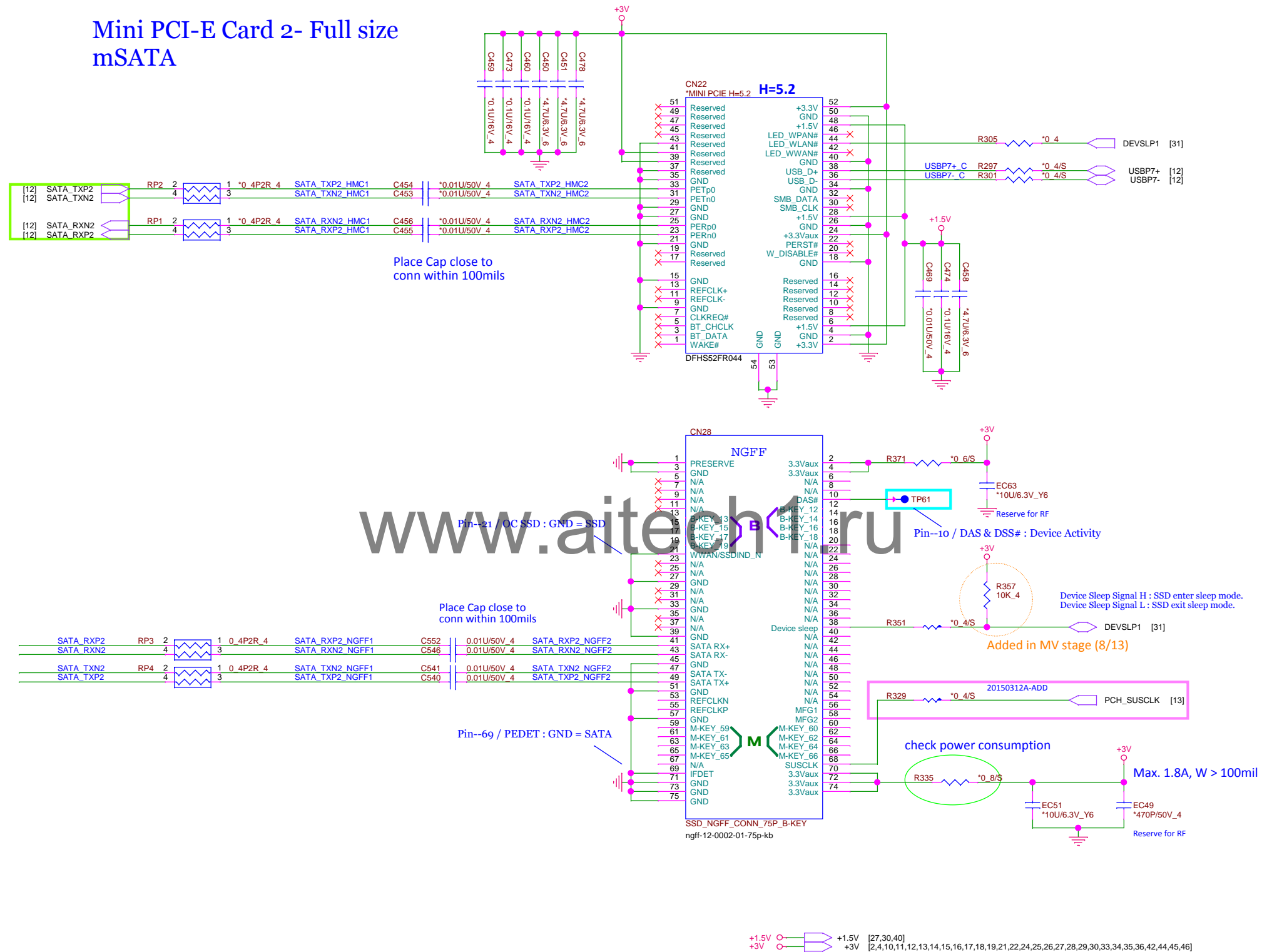
WIFI_DISABLE_L disable Antenna from PCH?

WLAN_OFF_L : Follow Yo7 control by EC.



FMC/iSATA

Mini PCI-E Card 2- Full size
mSATA



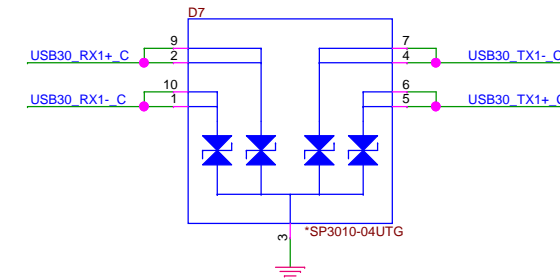
Follow TWE
2280/2242

Input Voltage	Parameter	32GB	64GB	128GB	256GB	512GB
SATA 6Gb/s host interface						
5V ± 5%	Read [mW]	NA	2,600	2,700	2,900	TBD
	Write [mW]	NA	2,200	3,350	4,800	TBD
3.3V ± 5%	Read [mW]	2,200	2,450	2,650	2,650	NA
	Write [mW]	2,100	2,150	3,400	4,500	NA

Table 3-3: SanDisk SSD X110 Average Max Power Consumption

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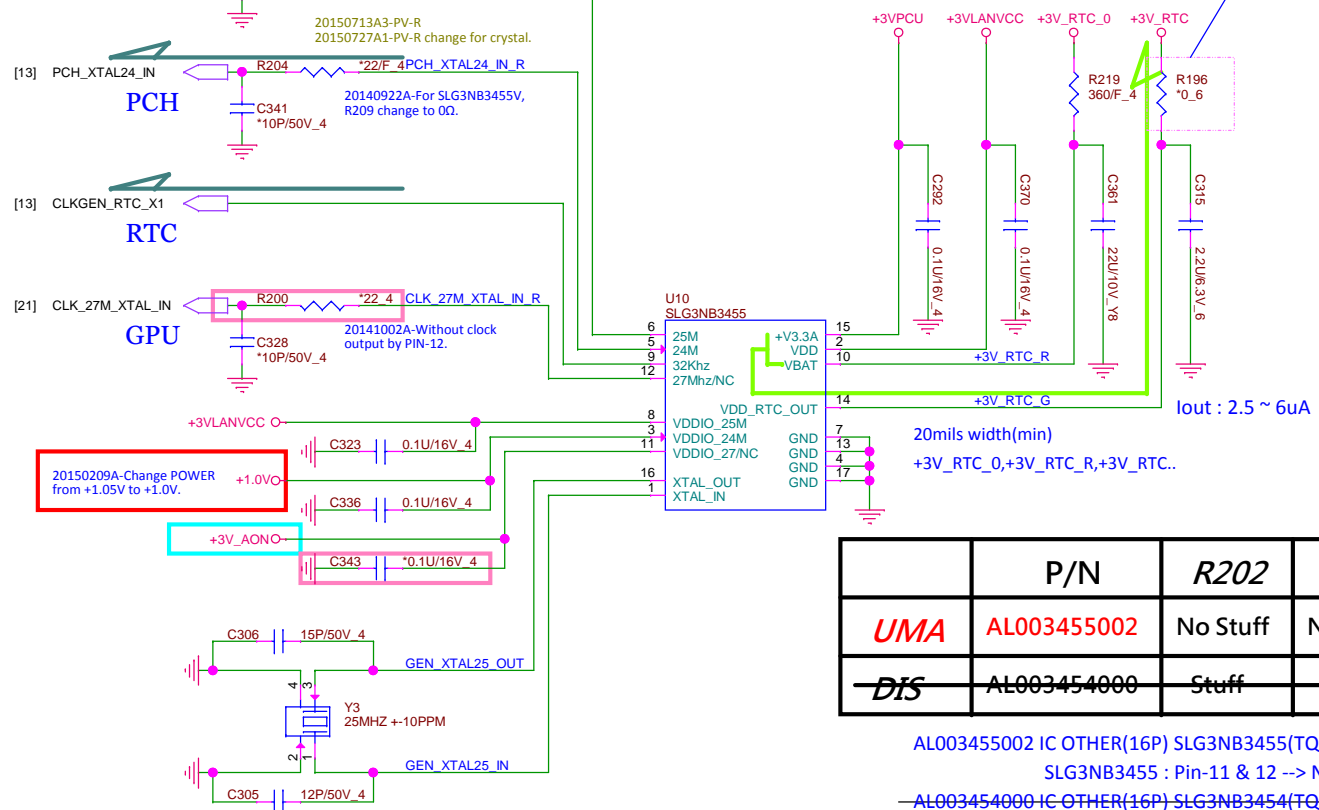
CAP CHIP 150U
6.3V(20%,ESR35,3528,H1.9)



The diagram shows four horizontal signal traces with components connected to them:

- LAN Section:**
 - Signal: LAN_XTAL25_IN
 - Component: R209 (pink box)
 - Value: 33 4
 - Label: LAN
 - Component: C367 (blue box)
 - Value: *10P/50V_4
 - Notes: 20150713A3-PV-R, 20150727A1-PV-R change for crystal
- PCH Section:**
 - Signal: PCH_XTAL24_IN
 - Component: R204 (pink box)
 - Value: **22F 4
 - Label: PCH
 - Component: C341 (blue box)
 - Value: *10P/50V_4
 - Note: 20140922A-For SLG3NB83455V, R209 change to 00.
- RTC Section:**
 - Signal: CLKGEN_RTC_X1
 - Label: RTC
- GPU Section:**
 - Signal: CLK_27M_XTAL_IN
 - Component: R200 (pink box)
 - Value: **22 4
 - Label: GPU
 - Component: C328 (blue box)
 - Value: 20141002A-Without clock

Green CLK Circuitry



	P/N	R202	C300
<i>UMA</i>	AL003455002	No Stuff	No Stuff
<i>DIS</i>	AL003454000	Stuff	Stuff

AL003455002 IC OTHER(16P) SLG3NB3455(TQFN)
SLG3NB3455 : Pin-11 & 12 --> NC.
~~AL003454000 IC OTHER(16P) SLG3NB3454(TQFN)~~

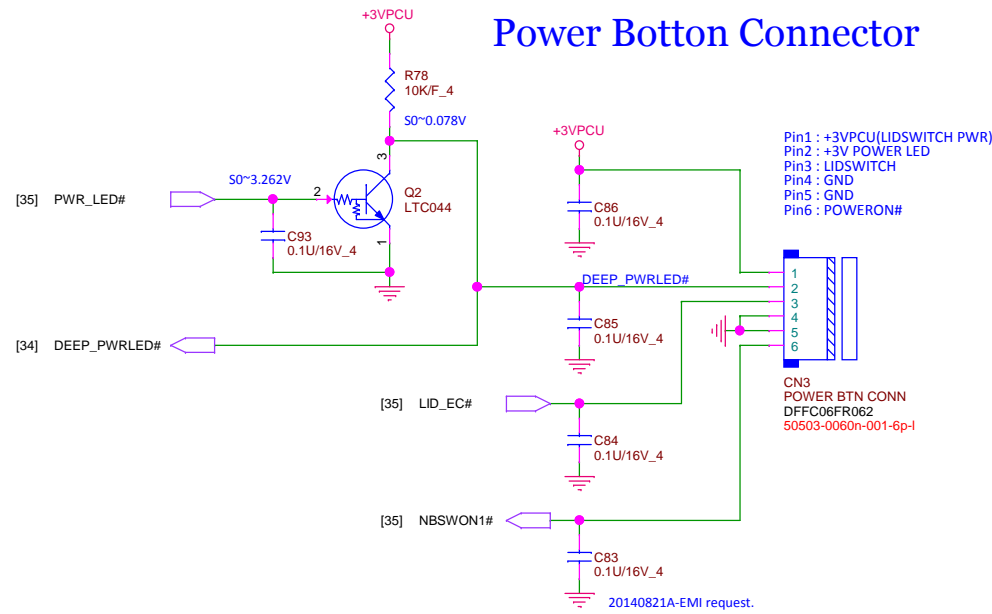


PROJECT : TWL & JWL (MB)

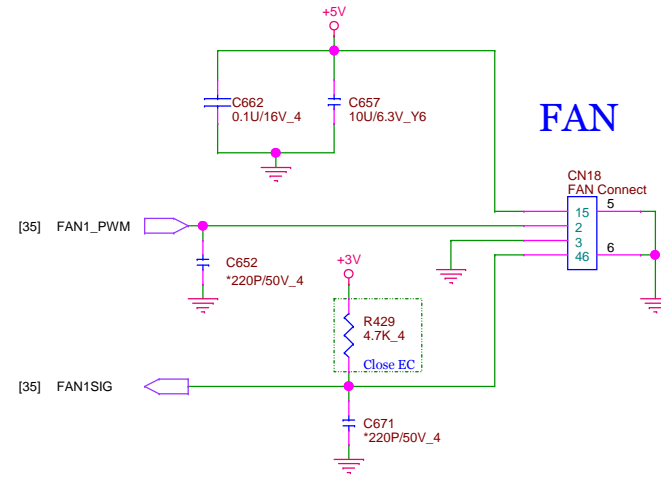
Size C	Document Number IC-USB3.0/G-CLK	Rev. 3C
Date: Wednesday, July 29, 2015	Sheet : 32 of 51	

0327 :
DEL Touch Pad Connector CN7 for U83
0927
Change CN4 PIN2 from +3V to DEEP_PWRLED# for Power LED

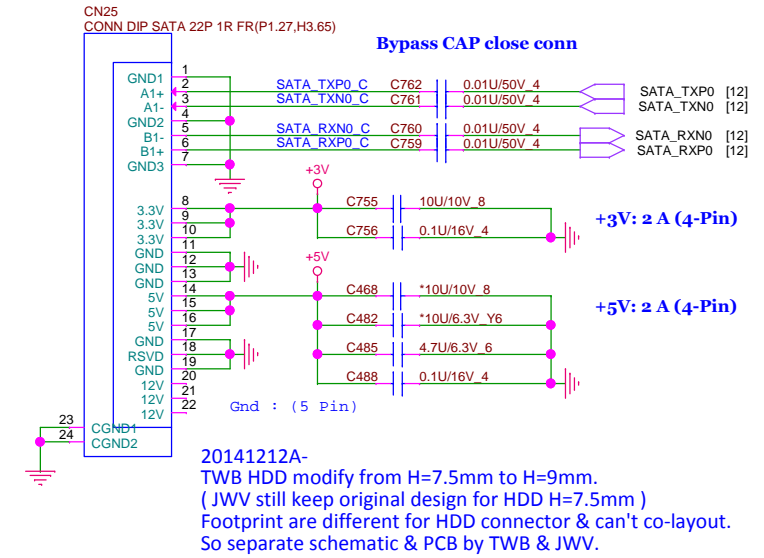
Power Button Connector



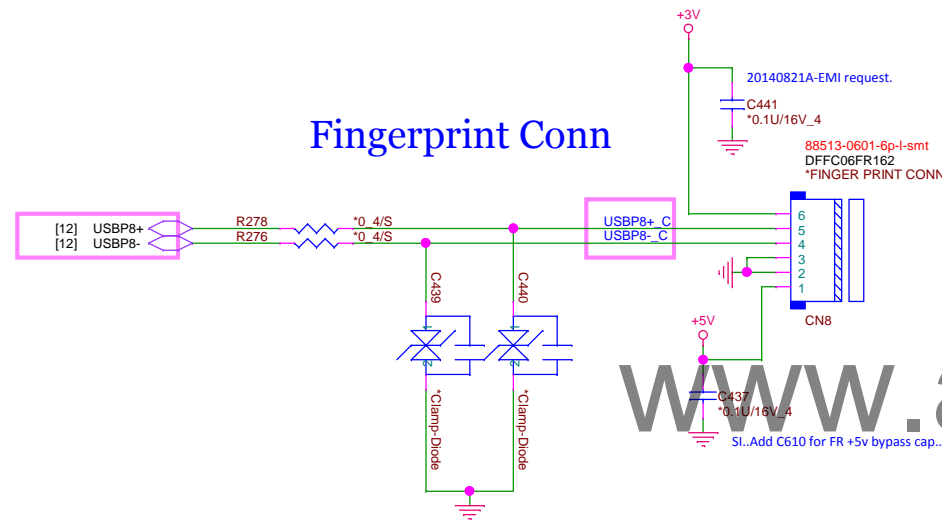
FAN



SATA HDD Connector



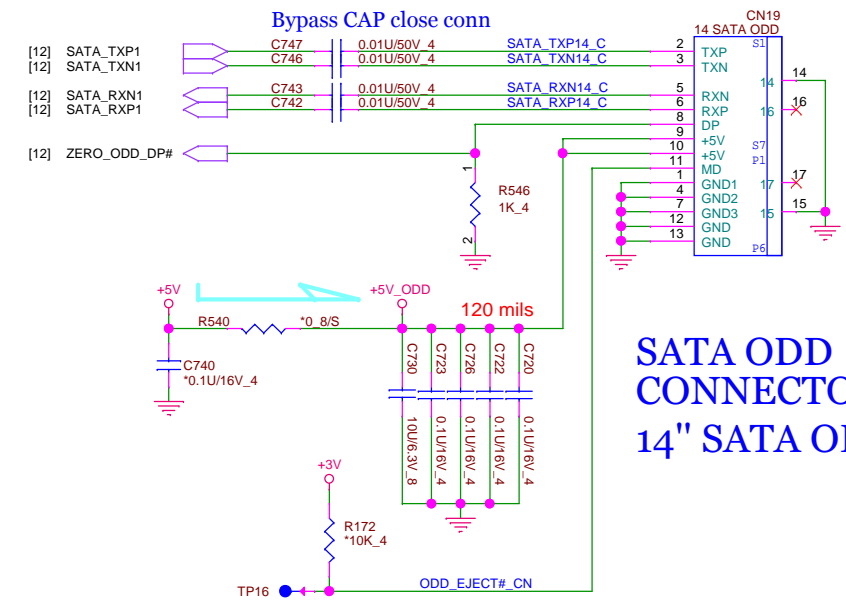
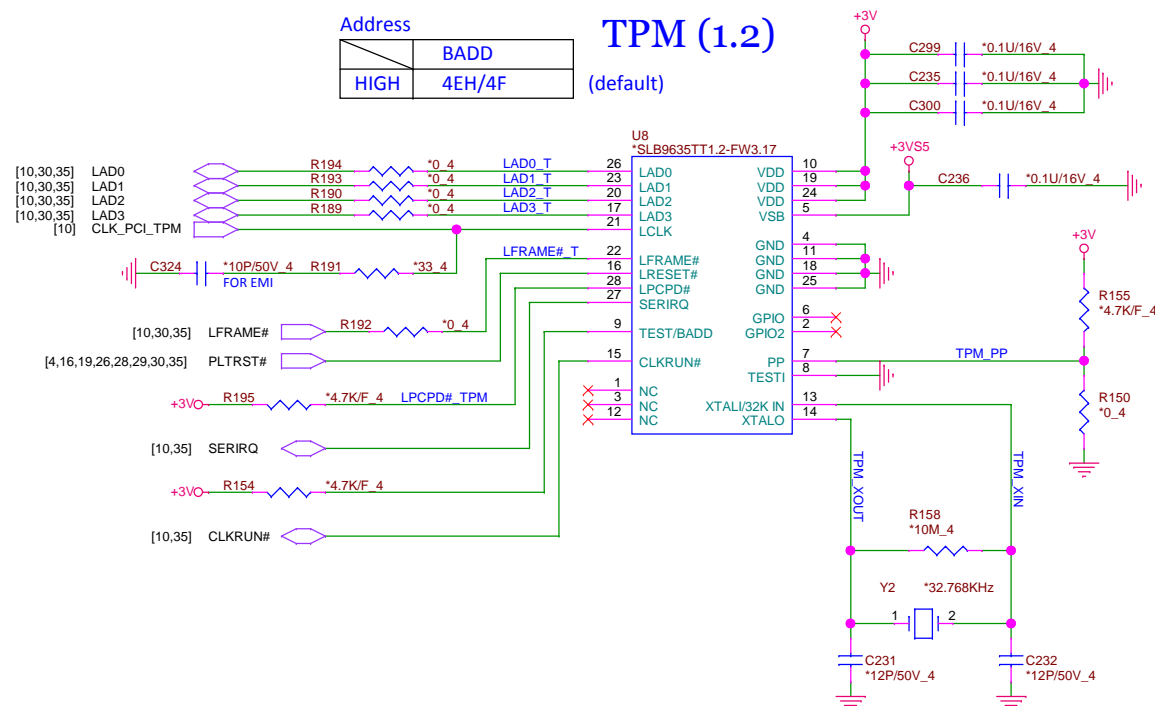
Fingerprint Conn



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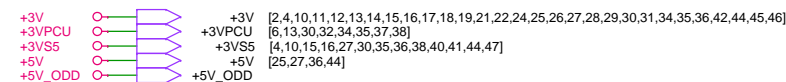
TPM (1.2)

Address	BADD
HIGH	4EH/4F (default)



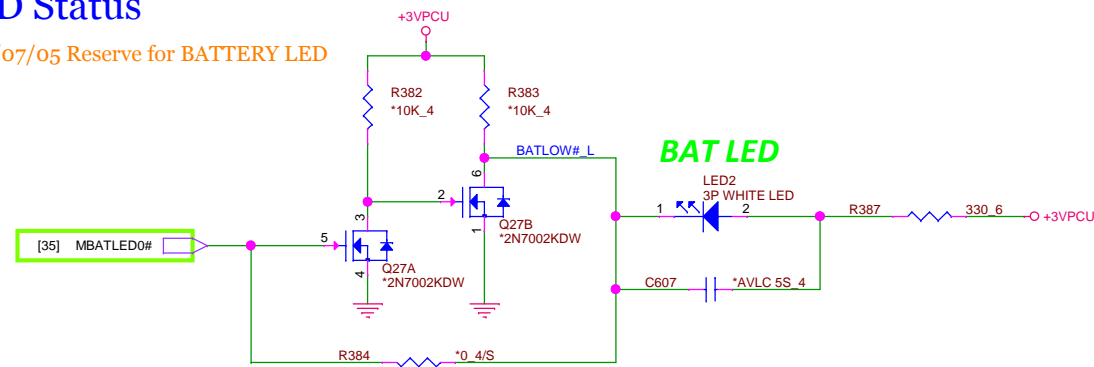
SATA ODD CONNECTOR 14" SATA ODD

JWV remove G-sensor/Touch Screen function.

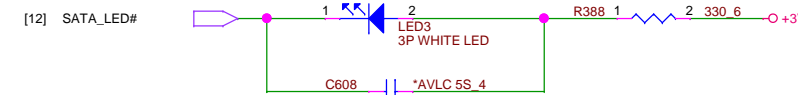


LED Status

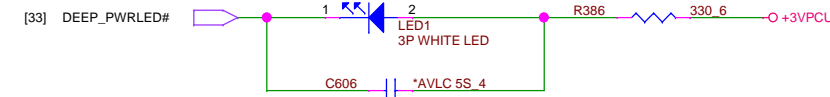
2013/07/05 Reserve for BATTERY LED



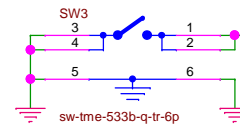
SATA LED



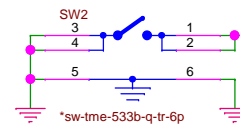
PWR LED



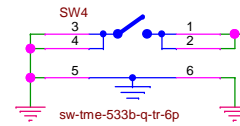
TWL 15" Left SW



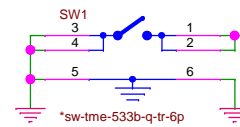
JWL 14" Left SW



TWL 15" Right SW



JWL 14" Right SW

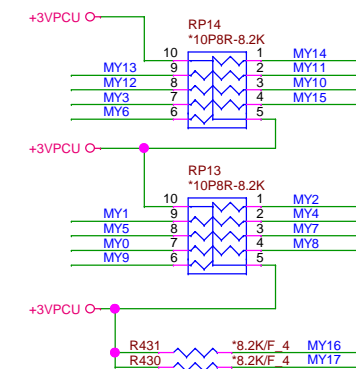
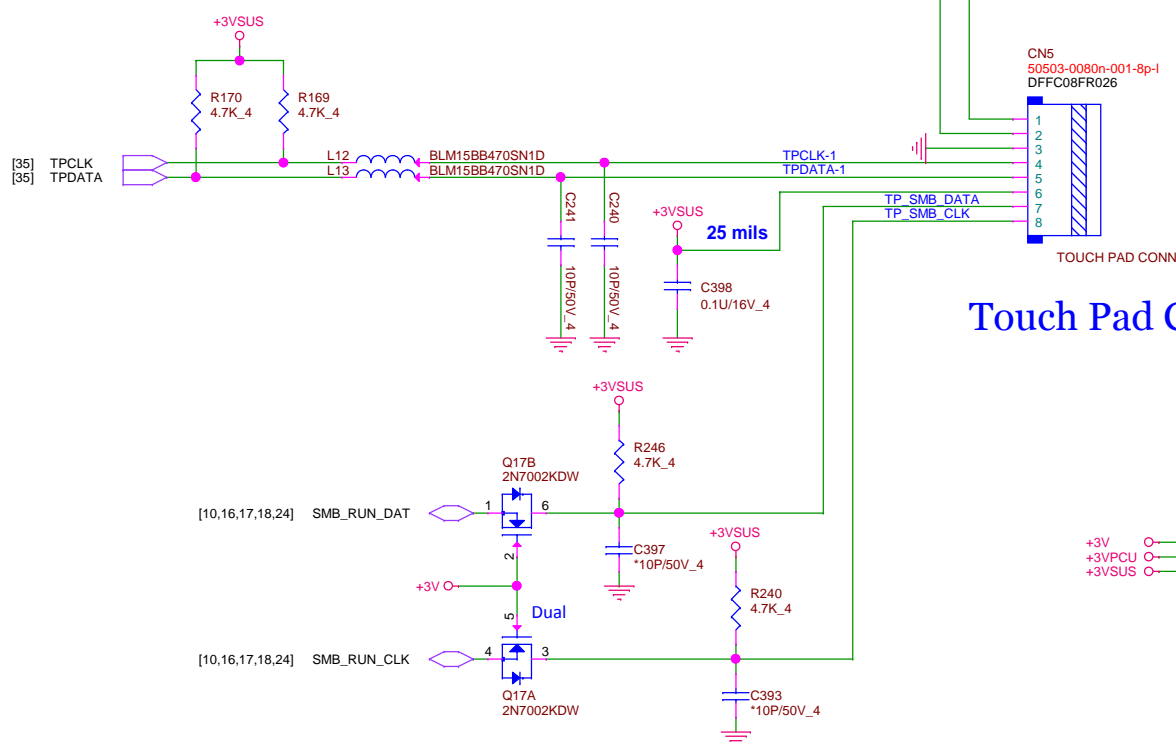
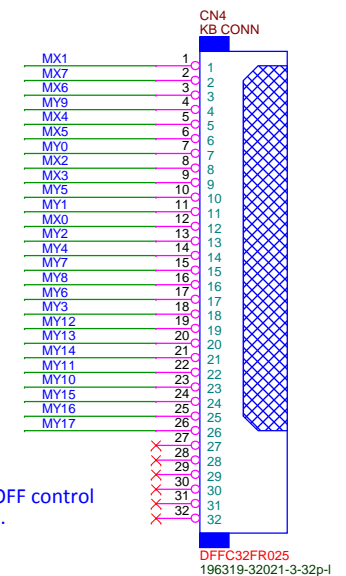


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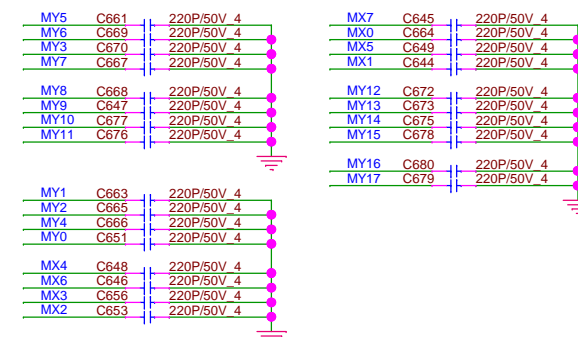
KEYBOARD CONN

0503 :
Change pin define and M/B keyboard connector follow R33

KEYBOARD PULL-UP

20150216A-
Cancel CAPSLED, MUTELED, WLAN ON/OFF control
for meet K/B function & reduce EC GPIO.

Touch Pad Connector

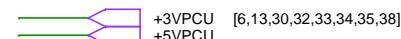
+3V
+3VPCU
+3VSUS

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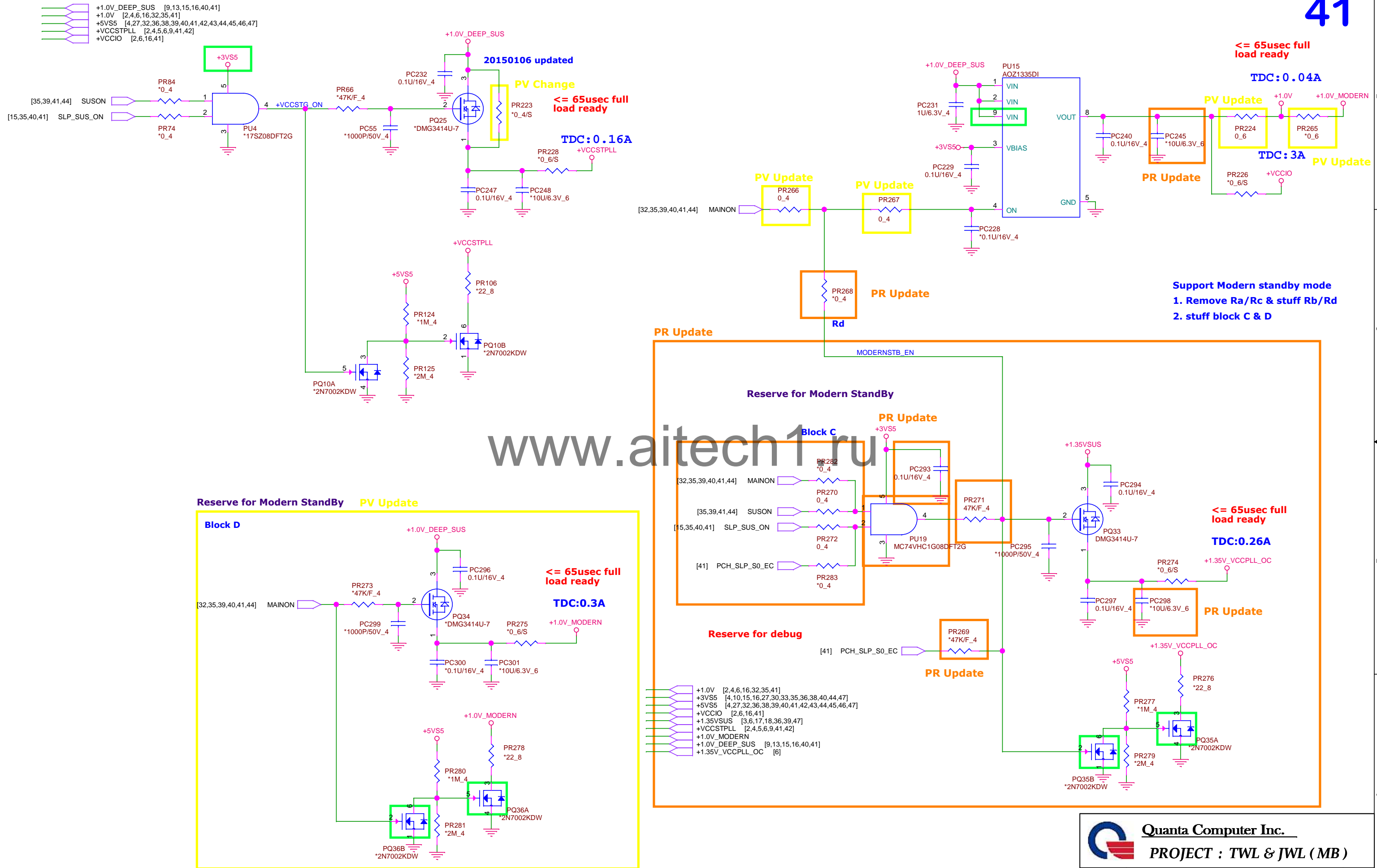
Size	Document Number	Rev.
C	CN-LED/KB/TP Button	3C
Date:	Wednesday, July 29, 2015	Sheet : 34 of 51

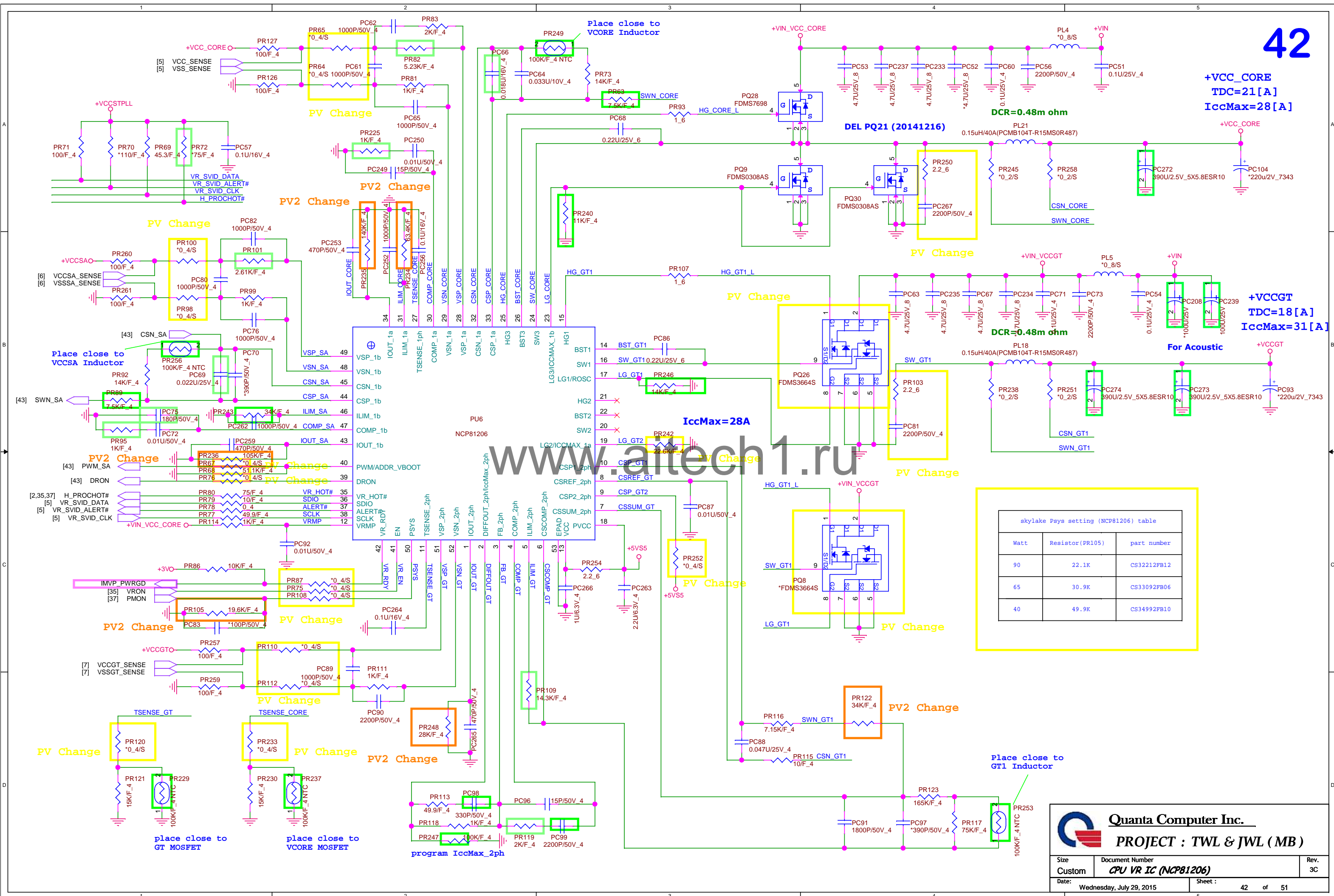


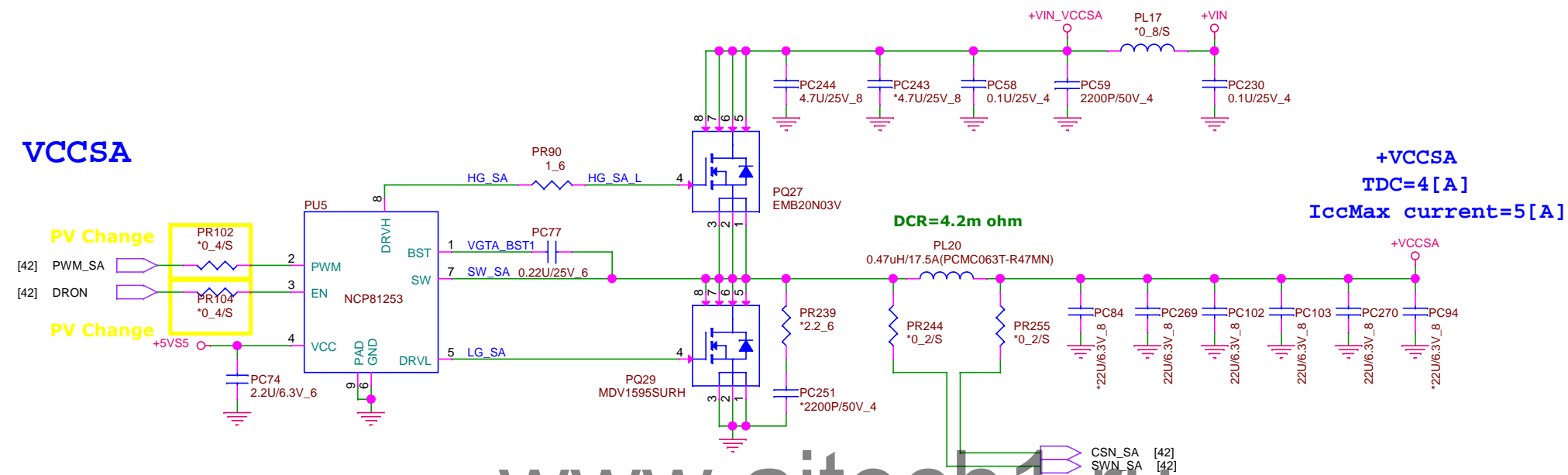


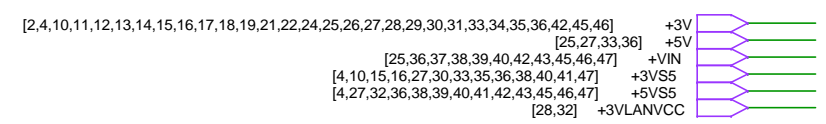
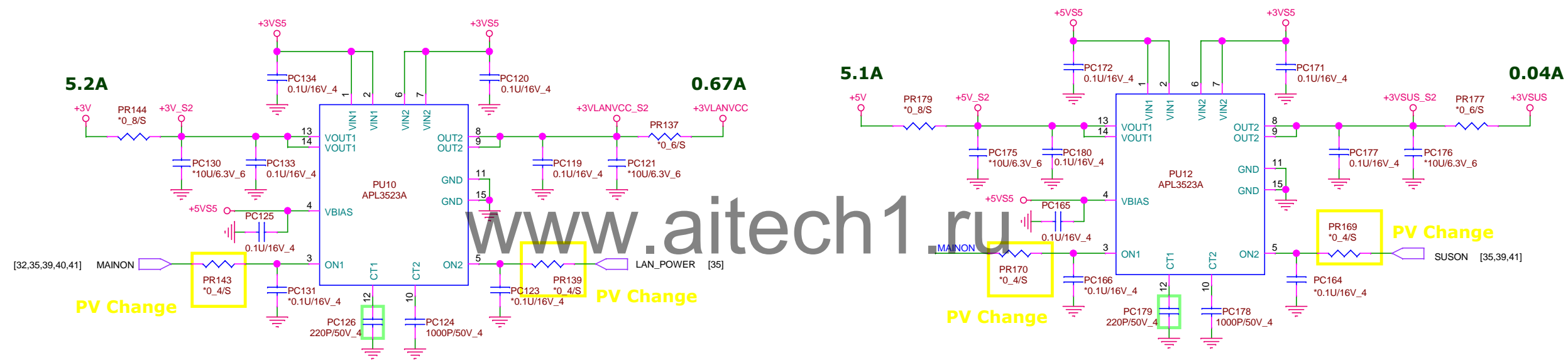


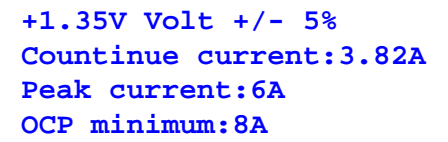
Size Custom	Document Number DDR3 (RT8231B)	Rev. 3C
Date: Wednesday, July 29, 2015	Sheet : 39 of 51	

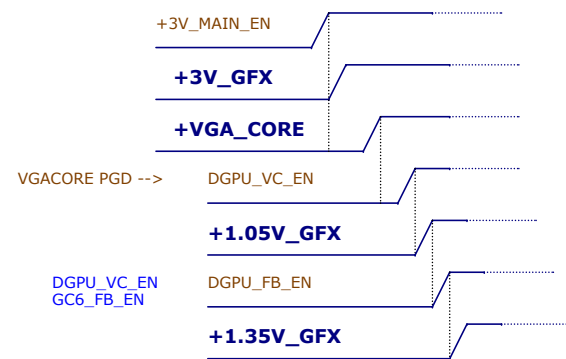




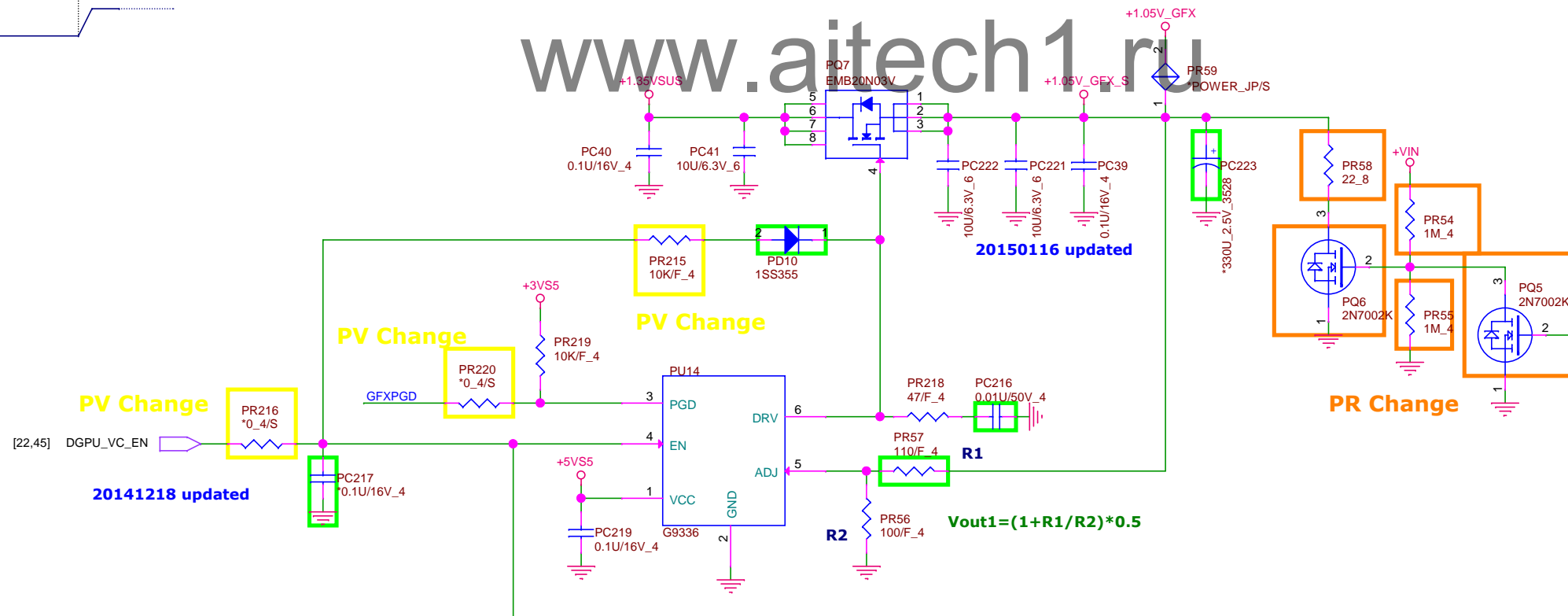


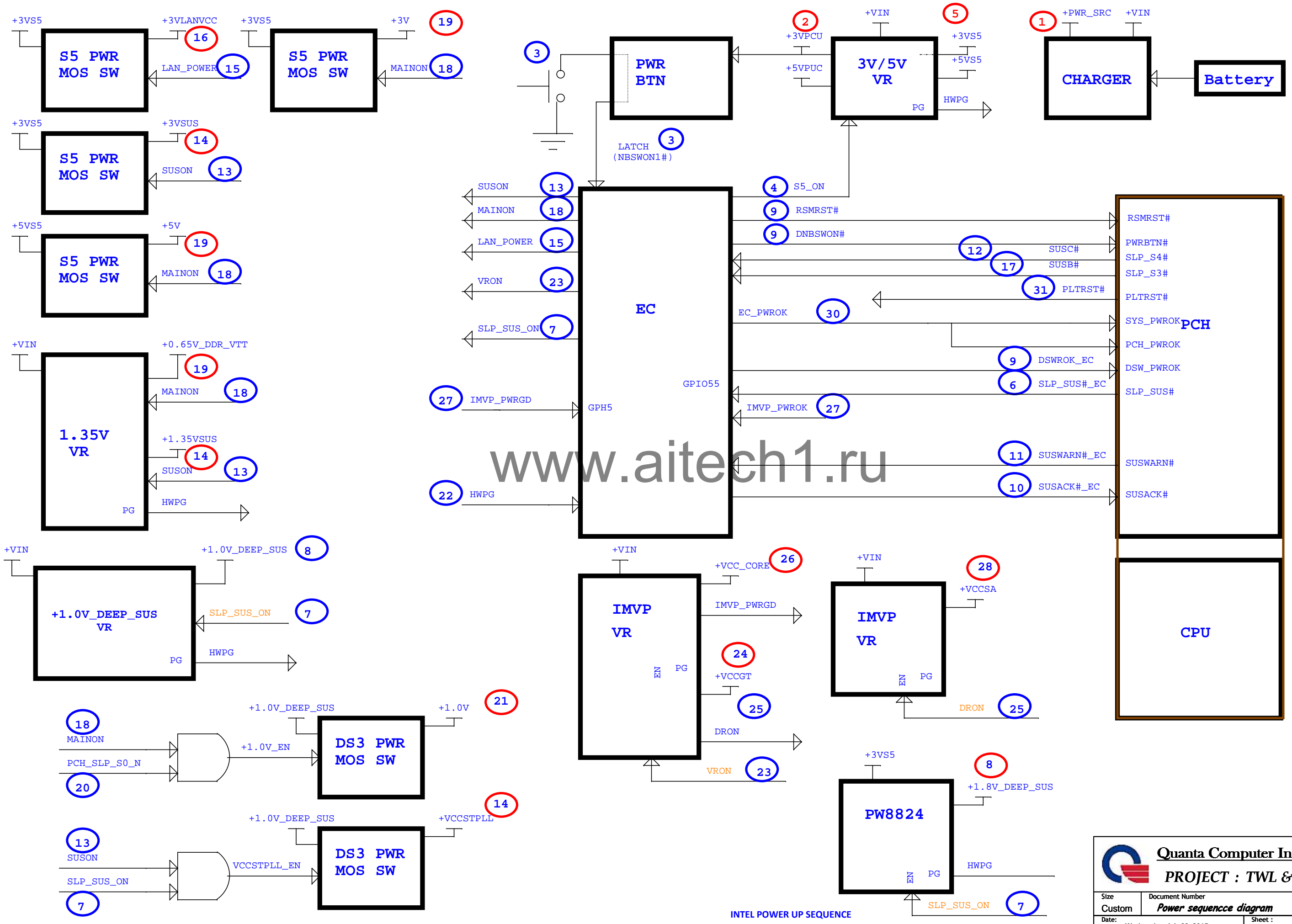


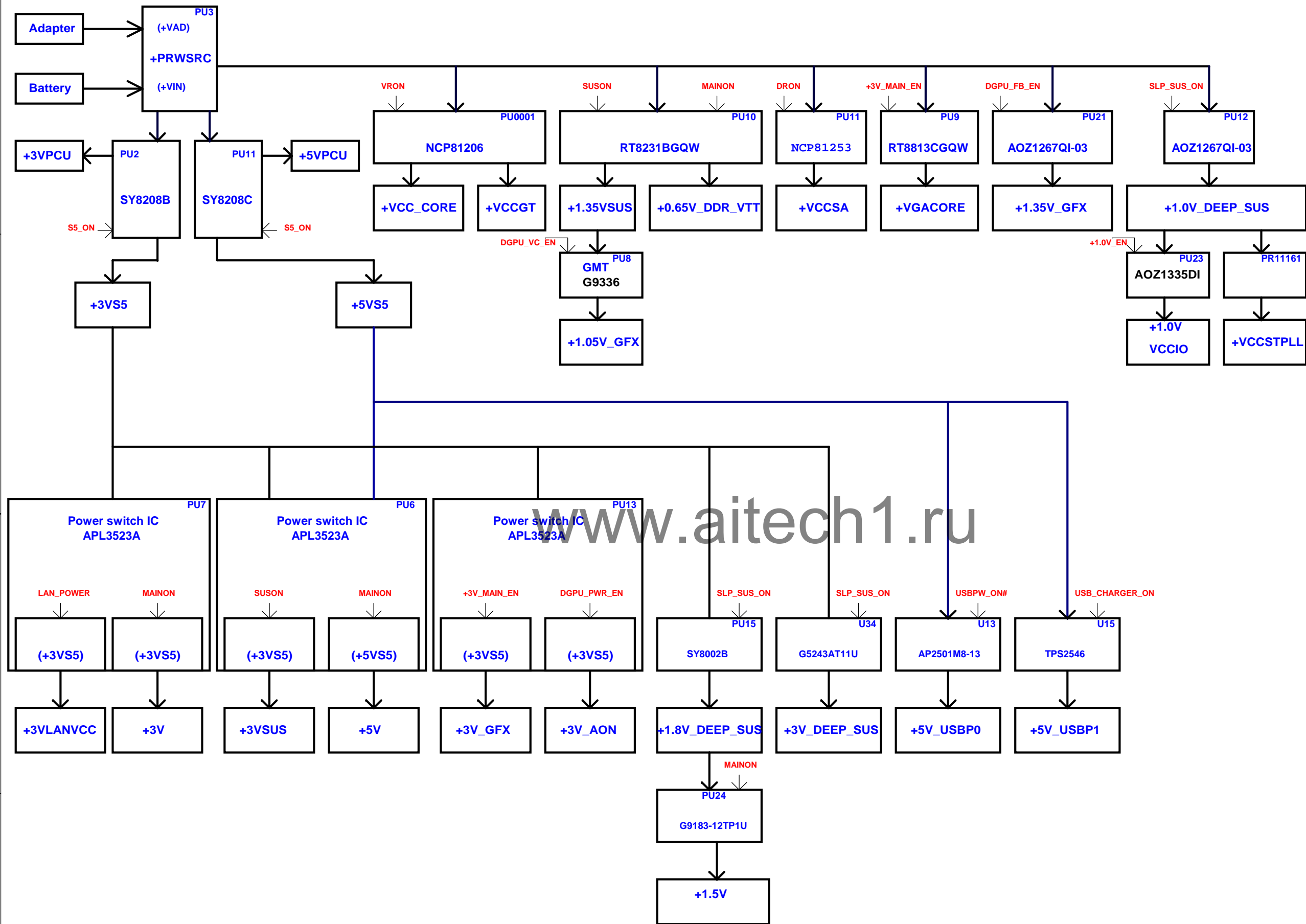




+1.05V_GFX +/- 5%
Countinue current:0.79A
Peak current:2.09A



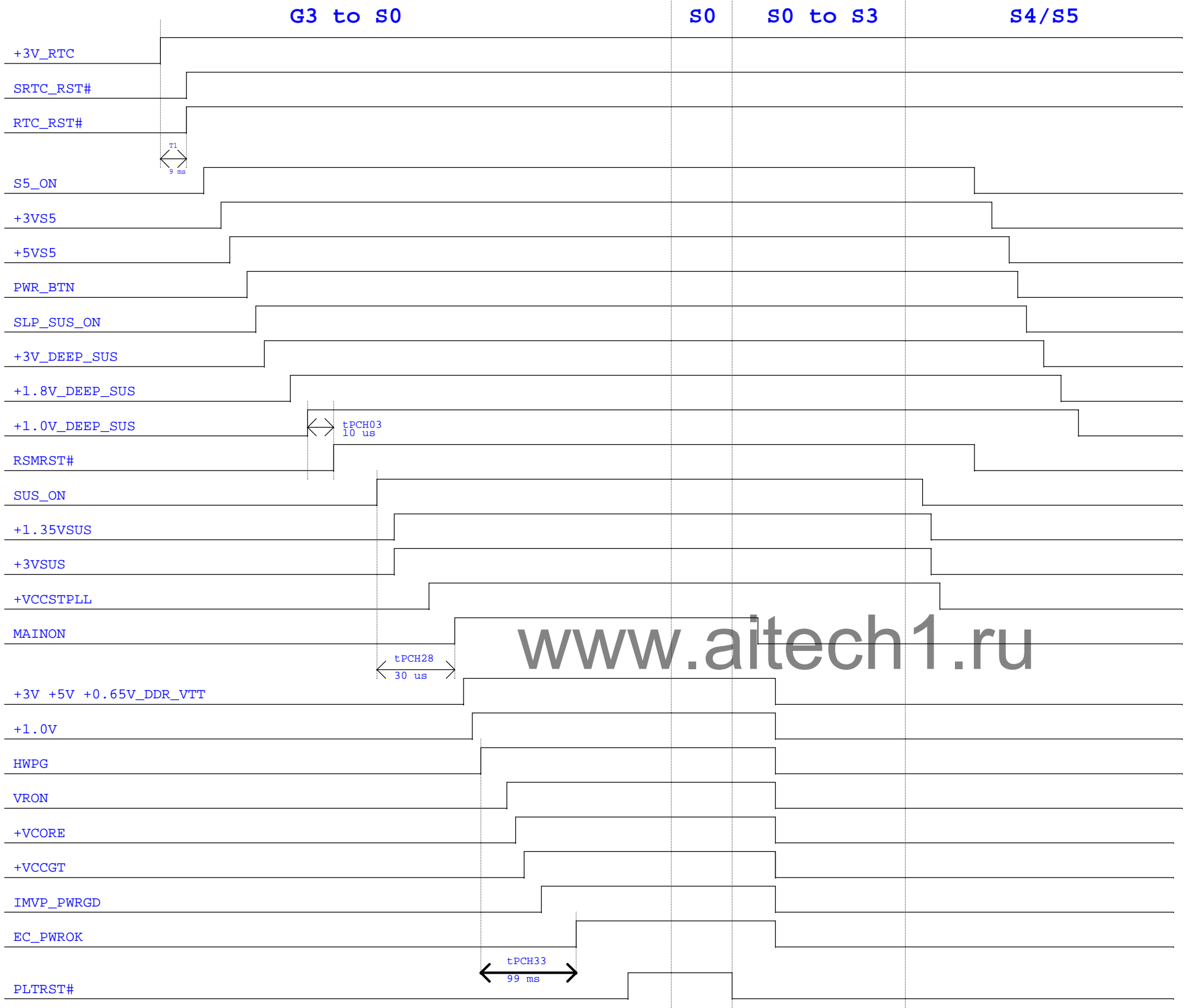




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Intel POWER UP SEQUENCE

TWL+JWL SYSTEM POWER BLOCK DIAGRAM

